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Over the three-year course of this program, the low-temperature-grown (LTG) GaAs and AlGaAs have been incorporated as the gate insulator or surface passivation in a variety of field-effect-transistors (FETs). The LTG GaAs used as the surface passivation layer in a metal-semiconductor FET (MESFET) with a novel overlapping gate structure increased the breakdown voltage by two folds compared to a regular MESFET. The LTG GaAs passivation also greatly improved the surface quality of the device, resulting in a reduced low-frequency noise and minimal frequency dispersions of the transconductance and the output resistance. The mechanisms for the improved breakdown voltage have been studied by computer simulation. Self-aligned GaAs metal-insulator-semiconductor FETs (MISFETs) having an LTG GaAs gate insulator have been developed. The performance of the MISFET was improved significantly by the ion-implanted high-doping-concentration source and drain regions. A variety of the LTG GaAs and LTG AlGaAs with different Al mole fractions, that can be used as the gate insulator, have been grown to study the effects of the growth temperature and the thickness on the properties of the MISFETs.

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1. INTRODUCTION

This is the final report for the program entitled "Investigation of GaAs Layers Grown by Molecular Beam Epitaxy at Low Temperature" which was undertaken from October 1, 1991 through September 30, 1994. At the beginning of this program, the low-temperature-grown (LTG) GaAs has just started been used as the gate insulator of a GaAs MISFET to improve the breakdown voltage. At the end of the three year period, the LTG GaAs has been successfully used as the passivation layer for MESFETs to increase the breakdown voltage and a self-aligned LTG GaAs MISFET has been developed for high-speed low-power-consumption applications.

2. PROGRAM OBJECTIVES

The objective of this program is to study the properties of the LTG GaAs under various growth and external annealing conditions and how the properties change of the LTG GaAs in a device will affect its characteristics. The work has been concentrated on the use of the LTG GaAs as the gate insulator and surface passivation layer of a FET-type device. A particular emphasis is placed on the improvement of the breakdown voltage and the gate leakage current of the FET.

3. ACCOMPLISHMENTS

3.1 DEVELOPMENT OF OVERLAPPING-GATE MESFET

A MESFET with LTG GaAs passivation and an overlapping-gate structure has been developed. The transconductance g_m is higher than that of an LTG GaAs MISFET because the gate is a Schottky contact instead of the MIS structure in the MISFET. However, the breakdown voltage of the new overlapping-gate MESFET is comparable to that of the MISFET. The overlapping-gate MESFET has been characterized carefully and a theory for the high breakdown is proposed based on computer simulations.

3.1.1 Fabrication of the Overlapping-gate MESFET with LTG GaAs passivation

In the LTG-GaAs development program proceeding to this one the LTG GaAs was used as the gate insulator in a MISFET which has achieved a gate breakdown voltage more

than double that of a conventional MESFET without surface passivation. It is speculated that the high breakdown voltage is the result of the presence of the high-resistivity LTG GaAs between the conducting channel and the gate-metallization near the drain-side. Since the electric field is the highest under the normal operation condition of a FET, a high gate-breakdown voltage can still be achieved even the MIS structure is form only at the edge of the gate. In an overlapping-gate MESFET, the drain current is controlled by the Schottky-contact portion of the gate, taking advantages of the more effective modulation of the conducting channel while the breakdown voltage is determined by the overlapping portion of the gate which is placed on top of the LTG GaAs passivation layer.

The overlapping-gate MESFET consists of a 1000-Å-thick GaAs active layer which is doped to 4×10^{17} cm^{-3} with Si. A 2000-Å-thick LTG GaAs was grown on top of the active layer as the surface passivation and another 2000-Å-thick LTG GaAs is under the active layer as the buffer. There is a 100-Å-thick AlAs layer between the GaAs channel and the LTG GaAs buffer as well as the passivation layers. All the layers were grown by molecular beam epitaxy (MBE) at 580 °C except for the LTG GaAs which was grown at 200 °C. A 1 μm gate was defined and the LTG GaAs passivation and the AlAs barrier in this area was etched to exposed the conducting channel. Then a gate overlay was patterned to lift off the gate metallization. The length of the gate overlap is approximately 0.2 μm on each side of the gate. A detailed description of the overlapping-gate MESFET can be found in Appendix A.

The g_m of the overlapping-gate MESFET is 136 mS/mm which is slightly higher than the 120 mS/mm for a control MESFET which has LTG GaAs passivation but without gate overlap. The breakdown voltage for the overlapping gate MESFET is 42 V which is very close to the 45 V breakdown voltage of a MISFET with the same dimensions. The unity-current-gain frequency f_T is 4.8 GHz for the overlapping-gate MESFET and 5.3 GHz for the control. The lower f_T is attributed to a slight increase in the gate capacitance due to the overlap. However, the contribution of the additional capacitance is small and this is also confirmed by the simulation which will be discussed in section 3.2. The values of the maximum frequency of oscillation f_{max} are 15.2 and 14.4 GHz for the overlapping-gate and control MESFET, respectively. This higher f_{max} could be caused by a higher output resistance R_{out} of the overlapping-gate MESFET.

It has been shown that the overlapping-gate MESFET with LTG GaAs passivation has a much improved breakdown voltage while the high-frequency performance is comparable to a conventional MESFET.

3.1.2 Dependence of the Breakdown Voltage on the Gate Overlap

It has been shown that using an overlap gate structure can significantly increase the gate breakdown voltage of a MESFET. The goal of this experiment is to investigate whether the length of the gate overlap would affect the breakdown voltage.

A new mask set which consists of MESFETs with varying length of gate overlap was designed. The length of the overlap ranges from 0 to 1.2 μm while the length of the Schottky contact portion of the gate was kept at approximately 1.2 μm. The source drain spacing is 7 μm for all the devices. The breakdown voltage is 43 V when there is no gate overlap and reaches the highest value of 52 V with a 0.6-μm gate overlap. Beyond this point the breakdown voltage begins to decrease with increasing overlap and measures 45 V at 1.2-μm overlap. For comparison, LTG GaAs MISFETs, in which the entire gate metallization is on the LTG GaAs, were also fabricated on the same wafer. With a fixed gate length, the breakdown voltage increases monotonically with the spacing between the edge of the gate and the ohmic contact.

For the MESFET with 0.6 μm gate overlap, the spacing between the edge of the overlapping portion of the gate and the ohmic contact is 1.9 μm and the breakdown voltage of the MISFET with 1.9-μm gate-drain spacing is 49 V which is close to the 52 V for the MESFET. For MESFETs with gate overlap more than 0.6 μm the breakdown voltage is very close to the breakdown voltage of the MISFETs with the same gate-ohmic spacing. The following conclusions were drawn from this study: (1) Gate overlap increases the breakdown voltage. (2) The breakdown voltage increases with the length of the overlap but the rate of increase drops significantly beyond approximately 0.2-μm of overlap. (3) The breakdown in an overlapping-gate MESFET takes place at the overlapping portion of the gate instead of at the Schottky contact. (4) When the edge of the gate becomes too close to the ohmic contact (~ 1.9 μm in our devices) the breakdown voltage of both the overlapping-gate MESFET and MISFET is determined mainly by the spacing between the gate and the ohmic contact.

3.1.3 Stability of MESFETs with LTG GaAs passivation

Because in an overlapping-gate MESFET portions of the gate metallization are on the LTG GaAs which contains many traps and may introduce frequency-dependent properties. Because the g_m and R_{out} of a MESFET are sensitive to the traps at the surface of the conducting channel, these parameters vary with the frequency at which they were measured in accordance with the charge and discharge time constants of the traps.

In this experiment the frequency dispersion of g_m and R_{out} was measure on MESFETs having LTG GaAs surface passivation with and without gate overlap. For comparison, a conventional MESFET without surface passivation was also included as the control sample. The layer structure and the fabrication process for the MESFETs were discussed in the previous section. When the MESFET is biased in the drain-current saturation region, which is the common bias condition for an amplifier, the g_m variation of the LTG-GaAs passivated MESFET is smaller than that of the MESFET without surface passivation in the 20 Hz to 20 kHz frequency range tested. Actually, the g_m of the overlapping-gate MESFET shows no measurable change for the entire frequency change. The R_{out} of the overlapping-gate MESFET is much higher than that of the MESFETs with a conventional gate structure and does not vary with the frequency either.

It appears that the LTG GaAs is a good surface passivation layer. The overlapping-gate structure insures that there is no exposed channel surface and can further reduce the frequency dispersion phenomenon that is related to the surface traps. A more detailed description can be found in Appendix B.

3.1.4 Low-Frequency Noise of the MESFET with LTG GaAs Passivation

The phase noise and the low-frequency noise of a regular GaAs MESFET without surface passivation and an overlapping-gate MESFET with LTG GaAs passivation were compared. The two MESFETs have the same physical dimensions and channel doping concentration with differences only in the surface passivation and the gate structure. Because the type of the noise mentioned depends strongly on the traps at the surface of the conducting channel, this experiment provides information on the effect of the LTG GaAs passivation.

Both the low-frequency noise and phase-noise measured with 1-GHz carrier show that the noise of the overlapping-gate MESFET is much lower than that of the unpassivated MESFET. At 1 Hz offset frequency, the difference is more than 20 dB. The noise of the unpassivated MESFET follows closely the 1/f relation with the frequency. On the other hand, the noise fall-off of the overlapping-gate MESFET is more gradual, indicating the LTG GaAs change the characteristics of the traps at the surface of the conducting channel. With the same forward bias on the gate of the two MESFETs, the gate current of the overlapping-gate MESFET is slightly higher but the total noise associated with the gate current is lower, providing a quieter operation.

As described in Appendix C, the LTG GaAs passivation changes the surface traps characteristics and reduces the low-frequency and phase noise of the MESFET. Therefore, the overlapping-gate MESFET with LTG GaAs passivation is more desirable for applications such as oscillators which are very sensitive to the low-frequency noise.

3.2 THEORY FOR THE BREAKDOWN OF OVERLAPPING-GATE MESFET

The breakdown voltage of an overlapping-gate MESFET with LTG GaAs passivation is comparable to that of an LTG GaAs MISFET even though part of the gate metallization is placed directly on the highly-doped conducting channel. In order to explore the reasons behind it, computer simulations were used to study these devices. A two-dimensional device simulation program, BLAZE, has been acquired for this purpose.

The dimensions, such as the gate length and the channel thickness, were reduced from the actual devices fabricated to shorten the simulation time and ensure convergence. Since many variables, such as trap densities and the impact-ionization coefficients in the LTG GaAs, are unknown, it is not the intention of this work to match the simulation results with the experimental data. The goal is to understand the breakdown mechanisms and explain why the breakdown voltage of the overlapping-gate MESFET with LTG GaAs passivation is always higher than that of an LTG-GaAs passivated MESFET with a conventional gate structure. Since the breakdown voltage of the unpassivated MESFET is much lower than those just mentioned, it is also our intention to find out how the surface passivation affects the breakdown voltage and the requirements for a good passivation layer.

The device structures and the simulation results can be found in Appendix D and only a brief summary is discussed here. The most important factor of achieving a high breakdown voltage is to have an increasing depletion width at the surface of the conducting channel from the drain to the gate. In an overlapping-gate MESFET, the electric field originated form the overlapping portion of the gate widens the surface depletion region between the gate and drain. The highest electric field is shifted from the Schottky contact to the location directly under the edge of the overlapping portion of the gate. Since the LTG GaAs has a very high field strength, the breakdown voltage increases significantly. The surface passivation along can alter the field lines between the gate and the drain resulting an increased breakdown voltage, the planar nature of the regular gate structure makes this improvement less effective. Although any high-resistivity dielectric can be used as the surface passivation, the LTG GaAs appears to be the optimal choice because of its matched dielectric constant and it can be grown in situ to maintain the best interface quality. The gate capacitance increases slightly due to the gate overlap, resulting in a lower f_T. However, a higher output resistance and breakdown voltage should make up for the higher gate capacitance for high-power and high-efficiency applications.

3.3 SELF-ALIGNED LTG GaAs MISFET

The LTG GaAs MISFETs previously reported suffer relative high source and drain resistance because the same doped active layer is used for both the channel under the gate and the areas between the gate and the ohmic contacts. Lowering the source and drain resistance would increase g_m and reduce the knee voltage, making the LTG GaAs MISFETs ideal for high-speed and low-power-consumption applications because of their very low gate leakage current in both forward and reverse bias conditions. Instead of using complicated techniques, such as etch and overgrowth, a simpler self-aligned ion-implantation approach is taken. Self-aligned n^+ implantation has been widely used to reduce the source resistance of GaAs MESFETs in an integrated circuit (IC). A new issue associated with the LTG GaAs MISFET is whether the LTG GaAs would degrade dramatically during the implant-activation anneal and become unsuitable as the gate insulator.

The epitaxial layers consist of a 2500-Å-thick undoped GaAs buffer, a 2000-Å-thick n-type GaAs channel nominally doped to 8×10^{16} cm^{-3} with Si, a 200-Å-thick undoped AlAs barrier, an 800-Å-thick undoped LTG GaAs grown at 200 °C, a 200-Å-

thick undoped AlAs barrier, and a 200-Å-thick undoped GaAs cap. All the layers, except for the LTG GaAs, were grown at 600 °C. The main difference between this MISFET and those reported previously is the addition of an AlAs barrier layer on top of the LTG GaAs gate insulator. This AlAs barrier layer is essential to prevent out-diffusion of the excess As and thus maintain the high resistivity of the LTG GaAs layer. The 700-Å-thick W gate is used as the self-aligned implant mask

With the 700-Å-thick W gate as the self-aligned mask the source and drain regions were implanted with Si using one of the implant schedules. In one schedule, the energy was 30 keV and the total dose was 2×10^{13} cm^{-2}. For the other schedule (sample B), the energy was 50 keV and the total dose was 3×10^{13} cm^{-2}. The implanted samples were annealed at 800 °C for 10 s. A complete description of the layer structures and the fabrication process are discussed in Appendix E.

The sheet resistance of the channel between the gate and the ohmic contacts was reduced from 1700 Ω/square for the as-grown sample to 620 and 480 Ω/square for samples implanted at 30 keV and 50 keV, respectively. The maximum drain current of the MISFET increases from 65 mA/mm gate width (V_{gs} = +2 V) to 160 mA/mm (V_{gs} = +4 V) for the sample implanted at 30 keV and 160 mA/mm (V_{gs} = +6 V) for the sample implanted at 50 keV. The f_T also increases from 2.2 GHz to 5.7 and 7.4 GHz for these samples. The forward-bias gate current increased slightly for the implanted samples but the LTG GaAs gate can still support several volts of forward bias without drawing measurable gate current.

The first self-aligned LTG GaAs MISFET has been developed. The degradation of the LTG GaAs gate after the high-temperature is minimal. The improvement in the maximum current, g_m, and the f_T demonstrated the benefits of the n^+ implant which has been accepted as a manufacturable process. The success of this work opens the door to a new class of GaAs MISFET with the potential of being the ideal device for low-power and high-speed applications. The fabrication process is simple and is standard for GaAs IC's. Because there is no gate recess, the threshold voltage is determined mainly by the epitaxial growth, and good device uniformity can be expected.

3.4 STUDY OF THE LAYER STRUCTURES SUITABLE FOR IMPLANT-ACTIVATION ANNEALING

The properties of the LTG GaAs and LTG AlGaAs are known to vary with the growth temperature and are also expected to react differently with the post-implant high-temperature annealing. It is likely that a good insulator layer may degrade more severely upon the high-temperature annealing and becomes inferior to the material grown under different conditions. In this part of the work, MIS diodes with various LTG GaAs and LTG AlGaAs layers as the insulator were fabricated. The forward- and reverse-biased current of the diodes with and without the high-temperature annealing were compared.

In the first experiment, an 800 Å thick of either LTG GaAs or LTG $Al_{.31}Ga_{.69}As$ was used as the insulator of the diode. The insulator was sandwiched by 100-Å-thick AlAs layers which was grown at the normal temperature. The active layer under the insulator is 5000 Å thick and doped with Si to 5×10^{16} cm^{-3}. All the layers were grown on n^+ GaAs substrates. As described in Appendix F, 150-μm-diameter MIS diodes were fabricated by lifting off Ti/Au metallization.

Before an 800-°C 10-s rapid thermal annealing (RTA), a schedule commonly used for the implant activation, the MIS diode with an LTG $Al_{.31}Ga_{.69}As$ insulator grown at 300 °C has the lowest forward-biased current and is followed by the one with LTG GaAs grown at 200 °C. After the RTA the LTG $Al_{.31}Ga_{.69}As$ degraded dramatically and the lowest current was measured on diodes with the LTG GaAs grown at 200 °C insulator. The current of the diode with an LTG GaAs insulator grown at 350 °C is the highest with and without the RTA. If the AlAs barrier layer above the LTG insulator was removed, the amount of the current increase after the RTA is approximately twice as much as that with the AlAs barrier layer.

In the second part of the experiment the insulator was limited to the LTG AlGaAs and the thickness was reduced to 300 Å. In addition to diodes having the LTG $Al_{.31}Ga_{.69}As$ grown at 300 °C, diodes with the LTG $Al_{.43}Ga_{.57}As$ having 43% of Al concentration (which gives rise to the highest direct-bandgap energy) grown at 300 and 250 °C were also fabricated. Without the RTA, the current of the diode with the LTG $Al_{.43}Ga_{.57}As$ insulator grown at 250 °C is significantly lower than the others. However, this is also the one that suffers the most degradation after the RTA. The diode with the LTG $Al_{.43}Ga_{.57}As$ insulator grown at 300 °C has the lowest current after the RTA. For comparison, diodes with a 300-Å-thick $Al_{.31}Ga_{.69}As$ grown at the normal 600 °C were also fabricated and the current of these diode did not show measurable increase after the RTA. However, in the range of 0 to 1.5 V of forward-bias measured, the current of the diode with the $Al_{.31}Ga_{.69}As$ grown at the normal 600 °C is approximately 1 to 2 orders of

magnitude higher than that of diodes with LTG $Al_{.31}Ga_{.69}As$ or LTG $Al_{.43}Ga_{.57}As$ grown at 300 °C.

In summary, the dependence of the forward-bias diode current on the high-temperature annealing varies widely with type of the LTG insulator. If high-temperature annealing is required in the process, the LTG GaAs grown at 200 °C or the LTG $Al_{.43}Ga_{.57}As$ grown at 300 °C yields the lowest leakage current when they are used as the gate insulator. On the other hand, if no annealing is required for device fabrication, the $Al_{.43}Ga_{.57}As$ grown at 250 °C is the insulator provides the lowest current.

4. PROFESSIONAL PERSONNEL

Over the course of this program, the following personnel were involved in the research effort.

NAME	CONTRIBUTION
C.L. Chen	Device design, fabrication, testing, and analysis
L.J. Mahoney	Device fabrication, process development
K.B. Nichols	MBE growth
M.J. Manfra	MBE growth
A.R. Calawa	Material development
R.A. Murphy	Device development
E.R. Brown	Device development

Abstract

Over the three-year course of this program, the low-temperature-grown (LTG) GaAs and AlGaAs have been incorporated as the gate insulator or surface passivation in a variety of field-effect-transistors (FETs). The LTG GaAs used as the surface passivation layer in a metal-semiconductor FET (MESFET) with a novel overlapping gate structure increased the breakdown voltage by two folds compared to a regular MESFET. The LTG GaAs passivation also greatly improved the surface quality of the device, resulting in a reduced low-frequency noise and minimal frequency dispersions of the transconductance and the output resistance. The mechanisms for the improved breakdown voltage have been studied by computer simulation. Self-aligned GaAs metal-insulator-semiconductor FETs (MISFETs) having an LTG GaAs gate insulator have been developed. The performance of the MISFET was improved significantly by the ion-implanted high-doping-concentration source and drain regions. A variety of the LTG GaAs and LTG AlGaAs with different Al mole fractions, that can be used as the gate insulator, have been grown to study the effects of the growth temperature and the thickness on the properties of the MISFETs.

Appendix A

High-Breakdown-Voltage MESFET with a Low-Temperature-Grown GaAs Passivation Layer and Overlapping Gate Structure

Chang-Lee Chen, *Member, IEEE*, Leonard J. Mahoney, Michael J. Manfra, Frank W. Smith, *Member, IEEE*, Donald H. Temme, *Member, IEEE*, and Arthur R. Calawa

Abstract—GaAs MESFET's were fabricated using a low-temperature-grown (LTG) high-resistivity GaAs layer to passivate the doped channel between the gate and source and between the gate and drain. The gate was fabricated such that the source and drain edges of the metal gate overlapped the LTG GaAs passivation layer. The electric fields at the edges of the gate were reduced by this special combination of LTG GaAs passivation and gate geometry, resulting in a gate–drain breakdown voltage of 42 V. This value is over 60% higher than that of similar MESFET's fabricated without the gate overlap.

I. Introduction

THE gate–drain breakdown voltage of a GaAs MESFET is one of the most important factors limiting its maximum output power. Methods to increase the breakdown voltage, such as a double gate recess and increased gate–drain spacing, are often accompanied by lower RF gain and/or drain saturation current. Attempts to increase the gate–drain breakdown voltage by placing an insulator between the gate metal and the MESFET channel usually introduce undesirable interface states. Recently, GaAs MISFET's with a low interface-state density were realized using a high-resistivity low-temperature-grown (LTG) GaAs layer as the gate insulator [1], [2]. A substantial increase in breakdown voltage has been achieved with LTG GaAs layers as thin as 500 Å.

The gate-breakdown mechanism is still not completely understood. It is generally believed that breakdown occurs at the gate edge nearest the drain where the electric field is highest or along the surface between the gate and drain [3]–[5]. The high breakdown voltage of the LTG GaAs MISFET has been attributed to a reduced electric field near the gate due to the presence of the high-resistivity LTG GaAs insulator. The LTG GaAs has the further advantage in that it apparently introduces negligible interface states [6].

Since the highest electric field occurs at the drain side of the gate edge, a high gate-breakdown voltage can still be achieved even if the MIS structure is formed only at the edge of the gate. We report the development of a GaAs MESFET with an overlapping-gate structure that has a breakdown voltage substantially higher than that of a conventional MESFET. The bottom of the Schottky-barrier gate contacts the channel as in a conventional MESFET, but both gate edges rest on LTG GaAs passivation layers. In this structure, parameters such as drain current and transconductance g_m do not differ from those of conventional MESFET's, and, in addition, it can be applied to other devices such as the high-electron-mobility transistor (HEMT).

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II. Device Fabrication

Schematic representations of the layer structures and cross sections of a conventional-gate MESFET and an overlapping-gate MESFET are shown in Fig. 1. Both devices have LTG GaAs surface passivation layers. The epitaxial layers, similar to those used for our LTG GaAs MISFET [2], were grown by molecular beam epitaxy and consist of a 2000-Å-thick LTG GaAs buffer layer, a 100-Å-thick AlAs layer, a 1000-Å-thick GaAs active layer doped with Si to 4×10^{17} cm^{-3}, a 100-Å-thick AlAs layer, and a 2000-Å-thick LTG GaAs layer. The growth temperature was 190°C for the LTG GaAs layers and 580°C for all other layers. Conventional-gate and overlapping-gate MESFET's were fabricated on respective wafers having this layer structure. Ohmic contacts were formed by first etching through the top LTG GaAs and AlAs layers and then depositing Ni/Ge/Au contact pads directly on the conducting n-GaAs layer.

On the wafer used for the MESFET with a conventional gate structure, the gate area was first defined by photoresist. The LTG GaAs and AlAs layers were then etched away in the gate opening and the conducting GaAs channel was recessed to obtain a drain saturation current I_{dss} of 200 mA/mm of gate width. Next, Ti/Au was evaporated and the gate was formed by a lift-off of the photoresist pattern.

On the wafer used for the overlapping-gate structure, the same gate mask as used above was used to define an opening for the removal of the LTG GaAs and AlAs layers for the channel-recess etch (again to an I_{dss} value of 200 mA/mm). This resist layer was removed after etching. A wider gate opening that overlaps the gate-recess region and the LTG GaAs top layer near the edges of the recess region was defined for the gate lift-off using a second layer of photoresist. The gate-recess length, drain–source spacing, and gate width were 1.5, 6, and 250 μm, respectively. Proton implantation was used for device isolation. The width of the gate

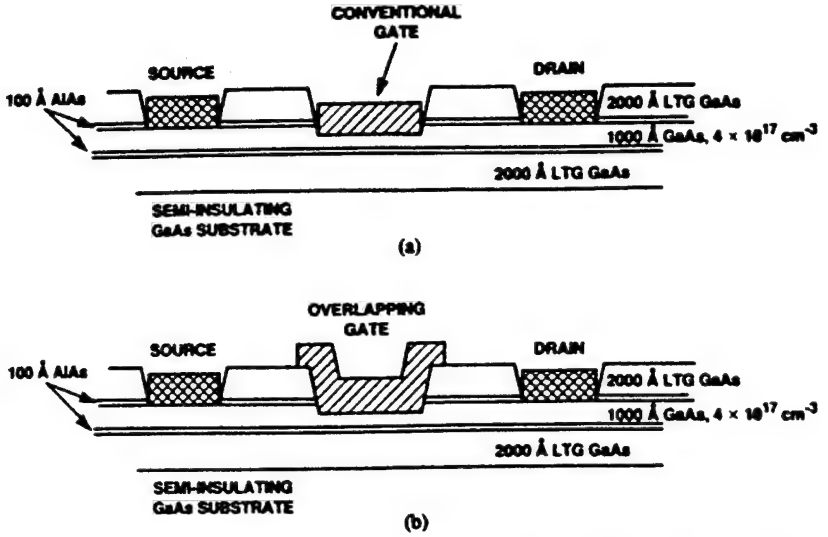

Fig. 1. Schematic diagram of the epitaxial layers and the cross sections of the gate structures of the two different MESFET's. (a) Conventional gate. (b) Overlapping gate.

overlap is less than 0.3 μm on either side of the gate recess. In one area on this wafer, the LTG GaAs and the conducting GaAs layers in the gate region were not etched, allowing MISFET's similar to those reported in [2] to be fabricated on the same wafer with the overlapping-gate MESFET's.

III. Results and Discussion

The I_{ds}–V_{ds} characteristics of the overlapping-gate MESFET are shown in Fig. 2. The 80-μs pulse mode of the curve tracer was used to reduce the heat generated by the device. Near pinchoff, there is no noticeable excessive drain current for V_{ds} as high as 35 V. The g_m values are 120 and 136 mS/mm for the conventional-gate and the overlapping-gate MESFET's, respectively. The higher g_m for the overlapping-gate MESFET may be due to the differences in gate structure or may be simply due to the difference in series resistance caused by process-related variations in ohmic contacts and gate–source spacing. With the overlapping-gate MESFET biased in the saturation region, the long-term drain current drift was less than 1% and no g_m dispersion was observed for frequencies between 20 Hz and 20 kHz.

The breakdown voltages for different devices are listed in Table I. The gate–drain breakdown voltage, defined at 200-μA/mm gate current, is 25 V for the conventional-gate MESFET and 42 V for the overlapping-gate MESFET. At pinchoff, the drain–source breakdown voltages for the conventional-gate and overlapping-gate MESFET's are 22 and 35 V, respectively. In contrast, the breakdown voltages for a standard MESFET fabricated with this same mask set but without an LTG GaAs passivation layer are 10 V for the drain–source breakdown and 15 V for the gate–drain breakdown.

The characteristics of the LTG GaAs MISFET fabricated on the same wafer used for the overlapping-gate MESFET are similar to those reported previously [7]. The forward gate turn-on voltage, also defined at 200 μA/mm of gate current, is 4.5 V for the MISFET compared to 0.4 V for the MESFET on the same wafer. The gate–drain breakdown voltage and drain–source breakdown voltage at pinchoff for the MISFET are 45 and 37 V, respectively. Compared to the overlapping-gate MESFET, the slightly higher breakdown

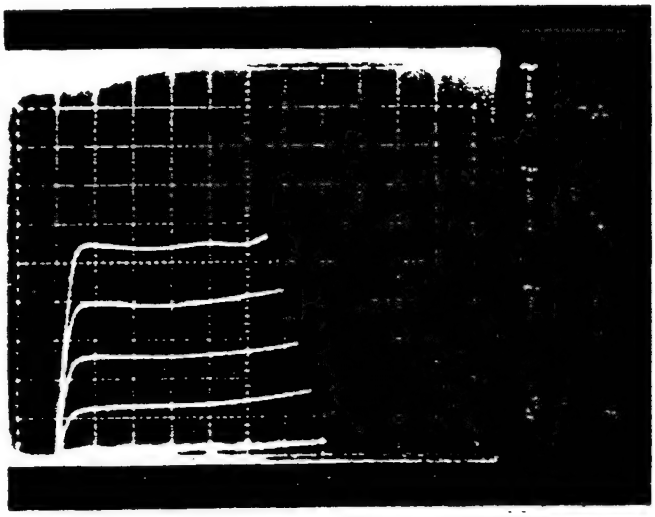

Fig. 2. The I_{ds}–V_{ds} characteristics of a MESFET with an overlapping gate. The gate voltage for the top curve is 0 V. The kinks in the top curve are believed to be caused by parasitics in the measurement setup which become important in the 80-μs pulse mode.

TABLE I
Breakdown Voltages for FET's

	LTG-GaAs-Passivated MESFET without Gate Overlap	LTG-GaAs-Passivated MESFET with Gate Overlap	LTG GaAs MISFET
Gate–Drain Breakdown (V)	25	42	45
Drain–Source Breakdown (V)	22	35	37

voltage in the MISFET is due to the added dielectric-breakdown voltage of the LTG GaAs gate-insulator layer itself.

Note that although the gate has a Schottky contact to the conducting channel in the overlapping-gate structure, the breakdown voltages are nearly equal to those of the MISFET, in which the entire gate metallization rests on a high-resistivity LTG GaAs layer. Apparently, the LTG GaAs in both structures eliminates the premature breakdowns in FET's. The mechanism for this effect is not clear. It is possible that the depletion region under the gate-overlap portion simply reduces the electric field at the gate edge.

The scattering parameters of these MESFET's were measured with $V_{ds} = 6$ V and $V_{gs} = 0$ V. The unity-current-gain frequency f_T is 4.8 GHz for the overlapping-gate MESFET and 5.3 GHz for the conventional-gate MESFET. The lower f_T is attributed to a slight increase in the gate capacitance. The values of maximum frequency of oscillation f_{max} are 15.2 and 14.4 GHz for the overlapping-gate and conventional-gate MESFET's, respectively. For $V_{gs} = -1.1$ V, the f_{max} of the overlapping-gate MESFET increased from 13.6 GHz for $V_{ds} = 8$ V to 15.1 GHz for $V_{ds} = 15$ V while f_T decreased from 4.7 to 4.2 GHz for the same voltage range. There was no unusual degradation at large V_{ds}. The drain current was biased at approximately half of the I_{dss} to minimize heating effects.

In a preliminary experiment for power measurement, an amplifier with eight overlapping-gate MESFET's connected in parallel (approximately 4-mm total gate width) was tested at 1.2 GHz. The amplifier was biased in class B and the output power increased with the drain bias. At $V_{ds} = 14$ V, the amplifier delivered 1.5 W of output power with 11 dB of gain and 46% of power-added efficiency. The estimated maximum voltage between the gate and the drain during the negative half-cycle of the input signal reached 33 V. The performance can be further improved by optimizing the impedance matching circuit of the amplifier, and by redesigning the device structure to reduce the source and drain resistances. The output power per unit gate width of the overlapping-gate MESFET is much higher than that of commercially available GaAs power MESFET's that we have measured using the same experimental setup. The commercial devices had a gate breakdown voltage of approximately 20 V, and hence could not sustain the same high drain bias applied to the overlapping-gate MESFET.

IV. Summary

A substantial increase in the breakdown voltage of a GaAs MESFET has been achieved by using an LTG GaAs surface passivation layer and a metal gate that overlaps the LTG GaAs layer at the edges of the gate. This increase in breakdown voltage was obtained without sacrificing drain current or gain and our measurements show no evidence of trap-related performance degradation. The breakdown voltage of such a MESFET is approximately equal to that of the LTG GaAs MISFET minus the gate forward turn-on voltage of the MISFET, this latter value being dominated by the dielectric-breakdown voltage of the LTG GaAs gate insulator. The overlapping-gate approach can be applied to any MESFET-like device, such as a HEMT, without interfering with the device active-layer structure. In addition to improving the breakdown voltage, the same LTG GaAs layer may also eliminate the need for further dielectric passivation. We believe it is possible that the high breakdown voltage can be preserved when the overlapped portion of the gate is shortened to reduce the gate capacitance. Studies are underway to optimize the overlapping-gate structure.

Acknowledgment

The authors would like to thank L. Cociani, D. J. Landers, and C. T. Harris for their technical support and M. A. Hollis for many helpful discussions.

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Appendix B

FREQUENCY DISPERSION OF TRANSCONDUCTANCE AND OUTPUT RESISTANCE IN GaAs MESFETs WITH LOW-TEMPERATURE-GROWN GaAs PASSIVATION LAYERS

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Indexing terms: Field-effect transistors, Transistors, Semiconductor devices and materials

High-resistivity GaAs grown at low temperatures by molecular beam epitaxy was used as the surface passivation layer of MESFETs. When these MESFETs are biased in the saturation region, the frequency dispersions of the transconductance and output resistance are reduced compared to those of a MESFET without a passivation layer.

Introduction: A good passivation layer for a GaAs MESFET should result in a MESFET with a high gate-breakdown voltage and low frequency dispersion in both transconductance g_m and output resistance R_{out}. We previously demonstrated that a high-resistivity low-temperature-grown (LTG) GaAs [1] layer on top of the conducting channel provides the desired high breakdown voltage [2]. We report here that MESFETs with an LTG GaAs passivation layer also have low frequency dispersion of g_m and R_{out} in the saturation region.

The layer is grown *in situ* by molecular beam epitaxy (MBE) and is lattice matched to the conducting channel. Therefore, the charge-trapping states at the surface of the conducting channel, which are the source of the dispersion, should be smaller in density than that observed with a dielectric passivation layer applied *ex situ* or with no passivation. Because the frequency dispersion characteristics of commercially available MESFETs vary widely depending on the layout, structure, and passivation of the device [3–5], a simple unpassivated MESFET having a structure and layout similar to those of the MESFETs with LTG GaAs passivation has been tested for comparison.

Experiments: The gate and layer structures of the MESFETs tested are shown in Fig. 1. The LTG GaAs passivation layers were grown by MBE at 190°C while the rest of the layers were

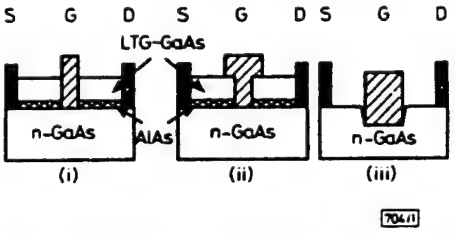

Fig. 1 *Cross-sections of standard-gate MESFET with LTG GaAs passivation, overlapping-gate MESFET with LTG GaAs passivation, MESFET without surface passivation*

The thickness of the top LTG GaAs and AlAs layers are 2000 and 100 Å, respectively.
(i) standard gate
(ii) overlapping gate
(iii) without surface passivation

grown at 580°C. The layers of the MESFET without passivation were grown by metal-organic vapour phase epitaxy (MOVPE). Because the dispersion is dominated by the surface properties of the conducting channel, the difference in epitaxial growth technique should have little effect on the dispersion characteristics. The fabrication processes are fairly standard for GaAs MESFETs and were reported in detail in Reference 2. The conducting-channel layer of the MESFETs passivated with the LTG GaAs was not intentionally recessed, whereas a 1000 Å gate recess was etched for the MESFET without the LTG GaAs top layer to obtain a drain current similar to that in the other devices. The influence of surface states should be more evident for the MESFETs without the gate recess. There was no additional dielectric layer on any of the MESFETs.

When a MESFET is biased below the point of drain-current saturation, the g_m dispersion observed can be attributed to variation both of the channel resistance directly under the Schottky gate and of the series resistances between the gate and source and between the gate and drain. The frequency dependence of these series resistances is dependent on the modulation of the space charge layer induced by the surface traps [3, 4]. When a more negative bias is applied to the gate, the channel resistance under the gate increasingly dominates the total resistance because of the large depletion width of the gate. Consequently, at high negative gate bias the relative frequency dispersion due to surface states decreases.

To study these effects, a sinusoidal signal with varying frequency is applied to the gate or the drain of the MESFET, and the corresponding drain-current signal is measured and used to calculate the frequency dispersion of g_m or R_{out}. The measurement setup is similar to that reported by Golio *et al.* [5], except that a digitising oscilloscope was used to replace the voltage meter. For all the experiments, the g_m or R_{out} was measured from 20 Hz to 20 kHz, and the amplitude of the applied signal was 0.2 V.

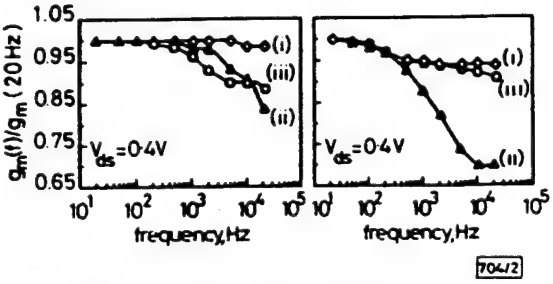

Fig. 2 *Measured g_m dispersion below saturation for $V_{gs} = 0$ V and for negative V_{gs} at which I_{ds} for each MESFET is approximately 15% of drain current at zero gate bias*

Labels on the curves refer to the structures of Fig. 1.
a $V_{gs} = 0$ V
b For $-V_{gs}$

In the g_m dispersion experiment, the MESFET was first biased below saturation with a drain voltage $V_{ds} = 0.4$ V. Two gate voltages were used for each MESFET, $V_{gs} = 0$ V and V_{gs} at which the channel is near pinchoff (i.e. where I_{ds} is approximately 15% of the drain current at zero gate voltage). The measured results in Fig. 2 show that for the MESFET without passivation, the normalised g_m(20 kHz)/g_m(20 Hz) increases from 0.885 at $V_{gs} = 0$ V to 0.912 near pinchoff. The dispersion for the standard-gate MESFET with the LTG GaAs passivation is smaller, and the normalised g_m actually decreases from 0.985 at $V_{gs} = 0$ V to 0.945 near pinchoff. The result indicates that the influence of the surface states in a MESFET with LTG GaAs passivation is less than that in a MESFET without passivation. A comparison with dielectric-passivated MESFETs [3, 4] also shows that the LTG GaAs passivation is more effective. In the overlapping-gate MESFET, the depletion region under the overlapping portion of the gate varies with the charging and discharging of traps in the LTG GaAs layer. Therefore, the dispersion of g_m is large, although the surface states outside the gate may contribute very little to the dispersion.

Next, the MESFET was biased in the drain-current saturation region, where the frequency dispersions of g_m and R_{out} are to the charging and discharging of the surface states above the portion of the depleted region that is extended beyond the gate electrode [5]. This charging and discharging change the width of the depletion region and the onset point of carrier-velocity saturation under the gate. The result of g_m dispersion in the saturation region is summarised in Table 1. The gate biases were chosen to keep I_{ds}, and therefore the power dissipation, approximately the same for all MESFETs. For the MESFET without passivation the g_m dispersion is less than that biased below the saturation region. By comparison, no dispersion is observed for the overlapping-gate MESFET, and g_m actually increases with increasing frequency for the

Table 1 VALUES OF g_m(20 kHz)/g_m(20 Hz) IN SATURATION REGION

MESFET structure	V_{ds} = 2·5 V	V_{ds} = 4·0 V
Standard-gate MESFET $V_{gs} = 2$ V	1·03	1·04
Overlapping-gate MESFET $V_{gs} = -0.5$ V	1·00	1·00
MESFET without passivation $V_{gs} = -2$ V	0·93	0·93

standard-gate MESFET with LTG GaAs passivation. As long as the MESFETs are biased in the saturation region, varying the drain bias has very little effect on the magnitude of the g_m dispersion.

In the saturation region, the R_{out} is more susceptible than the g_m to the charging and discharging of the surface states [5]. As shown in Fig. 3, R_{out} of the MESFET without passivation decreases more than 50% at $V_{gs} = 0$ V when the frequency increases from 20 Hz to 20 kHz. By comparison, for the standard-gate MESFET with LTG GaAs passivation the R_{out} increases slightly over the same frequency range, and the R_{out} of the overlapping-gate MESFET shows even smaller change with frequency.

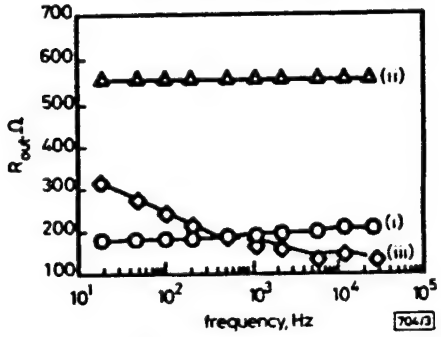

Fig. 3 *Measured R_{out} as function of frequency for $V_{ds} = 3$ V and $V_{gs} = 0$ V*

Labels on the curves refer to the structures of Fig. 1.

Conclusion: We have shown that in the saturation region, which is the bias condition for most MESFET applications, the g_m dispersion of MESFETs with the LTG GaAs passivation is less than that of a MESFET without passivation. In contrast to the case for the MESFET without surface passivation, the R_{out} of MESFETs with LTG GaAs passivation does not decrease when the frequency increases. Because g_m and R_{out} determine the voltage gain, the performance of MESFETs with LTG GaAs passivation layers will not deteriorate with increased operating frequency. Based on the dispersion results reported here and the high breakdown voltages already demonstrated, LTG GaAs is ideal for passivating the surface of GaAs MESFETs.

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Special Issue Paper

Appendix C

Low-Frequency Noise and Phase Noise in MESFETS with LTG-GaAs Passivation

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We report measurements of the low-frequency noise and phase noise of conventional unpassivated GaAs metal semiconductor field-effect transistors (MESFETs) and of MESFETs fabricated using an overlapping-gate structure and the low-temperature grown (LTG) GaAs as a passivation layer. The noise of the LTG-GaAs passivated MESFET was found to behave quite differently from that of a conventional MESFET and to be significantly reduced at low offset frequencies. These observations are explained in terms of the surface passivating effect of the LTG-GaAs. Low-frequency noise measurements seem to support the idea that the LTG-GaAs passivation reduces the number of active traps, in particular traps with large activation energies. These results indicate that LTG-GaAs passivation can substantially reduce the near-carrier phase noise of MESFET-based oscillators.

Key words: LT GaAs, noise, passivation

INTRODUCTION

Since the introduction of the low-temperature-grown (LTG) GaAs in 1988,[1] the interest in different applications of this material has been growing. Initially, it was used exclusively as a buffer layer between the substrate and the active layer in order to help reduce the effect of backgating. Later applications focused on increasing the gate-drain breakdown voltage[2] and on surface passivation.[3] Earlier noise measurements examined the influence of an LTG GaAs buffer on the low-frequency noise performance of metal semiconductor field-effect transistors (MESFETs)[4] and pseudomorphic heterojunction field-effect transistors.[5] In this paper, we focus on the effects of the LTG-GaAs on the low-frequency noise and phase noise of MESFETs when the material is used as a passivation layer on top of the conducting channel.

PHASE NOISE

An overlapping-gate MESFET with an LTG-GaAs passivation layer[3] (henceforth referred to as LTG-MESFET) and a conventional GaAs MESFET (henceforth referred to simply as MESFET) were used for the experiments. The 2000Å thick LTG GaAs passivation layer was grown in situ on top of the conducting channel by molecular beam epitaxy. No dielectric passivation layer was deposited to either the MESFET or the LTG-MESFET. The nominal gate length is 1 μm.

The phase noise of the devices was measured in the saturation regime using a 1 GHz carrier. The drain current was 60 mA and the drain-to-source voltage was 2.5 V. As illustrated in Fig. 1, the phase noise of the LTG-MESFET displays a flatter frequency dependence than the MESFET, which shows 1/f dependence, and is 15 dB lower at 1 Hz from the carrier and 10 dB higher at 100 kHz from the carrier. The lower near-carrier noise can be attributed to the passivation of surface states by addition of the LTG-GaAs layer. To test this assertion, we took low-frequency noise measurements on single devices when they were biased in saturation as well as the ohmic regime.

CHANNEL NOISE

The procedure for measuring low-frequency noise is standard and has been described elsewhere.[6] The

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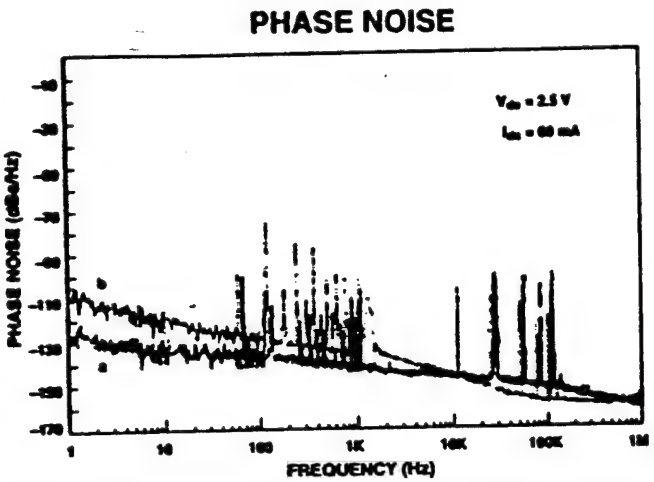

Fig. 1. Room-temperature phase noise measurements of devices biased in the saturation regime with I_{ds} = 60 mA: (a) LTG-MESFET, and (b) MESFET.

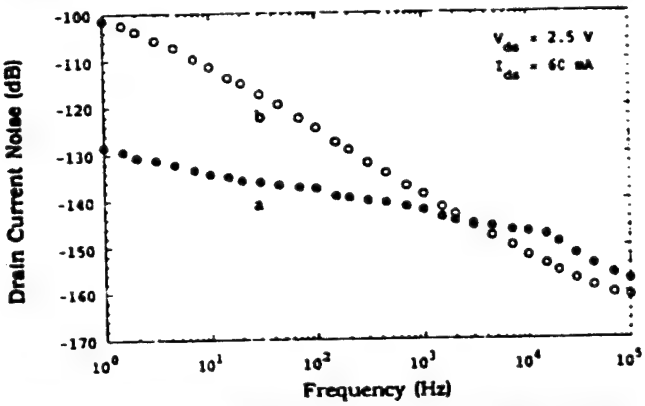

Fig. 2. Low-frequency noise of the same devices used in Fig. 1 for the phase noise measurement: (a) LTG-MESFET, and (b) MESFET.

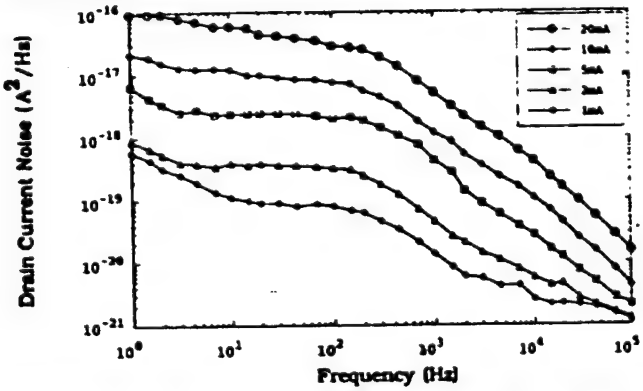

Fig. 3. Noise spectra of the LTG-MESFET in the ohmic regime for different drain currents. The gate-source voltage was kept constant at 0 V.

most noteworthy features of our technique are that it allows for amplifier noise and accounts for the nonflatness of the amplifier gain. In Fig. 2, we show the spectral intensity of the low-frequency drain-current fluctuations of the LTG-MESFET and MESFET in the saturation regime for a drain current of 60 mA and a drain-to-source voltage of 2.5 V. Two apparent differences between the devices are in the spectral shape and the magnitude of the noise. The MESFET exhibits a 1/f-shaped spectrum whereas the LTG-device has a weaker dependence on the frequency.

The low-frequency-noise measurements were consistent with the phase-noise results. At 1 Hz, the LTG-GaAs passivation reduced the phase noise and amplitude noise by 16 and 26 dB, respectively.

The low-frequency noise spectra for the LTG-MESFET biased in the ohmic regime are shown in Fig. 3. The gate bias was kept at 0 V while the drain current was varied from 0.5 to 10 mA. Further analysis identified two distinct spectral contributions: one (flat at small frequencies and rolling off at higher frequencies) that varies quadratically with the current (typical of a resistor) and may be associated with the conducting channel, and one (1/f-shaped and only observed at small frequencies and small currents) that varies linearly with current. The quadratic component has a frequency dependence that is weaker than 1/f and can in fact be modeled as a McWhorter-style[7] spectrum which is typical of a collection of trapping sites with a distribution proportional to the inverse of the trapping time constants:

$$S_i(f) = (A/f)\,[\arctan(f/f_1) - \arctan(f/f_2)],$$

where A is a constant proportional to the number of traps that are active, f the frequency, and $1/f_1$ and $1/f_2$ are the limits of the distritution of the trapping time constants. Such a spectrum is flat for frequencies smaller than f_1, rolls off as $1/f^2$ for frequencies larger than f_2, and behaves as 1/f for $f_1 < f < f_2$. The component that increases linearly with operating current can be modeled as having a 1/f dependence.

Similar measurements on the MESFETs in the ohmic regime reveal spectra that are almost perfectly 1/f-like and whose magnitude increases quadratically with increasing bias current. The fact that this component is not observed in the LTG-MESFETs leads us to believe that the 1/f noise is not fundamental in nature in the way described by Handel.[8] This component could not have been masked in the LTG-MESFETs because the observed noise is smaller than in the MESFETs. Hence, these 1/f shaped spectra could also be a manifestation of a McWhorter-style spectrum with a larger range of trapping time constants.

The difference between the MESFET and the LTG-MESFET is the addition of the LTG-GaAs passivation layer. It appears that the LTG-GaAs passivation layer modifies the distribution of the surface traps, resulting in a shift of the distribution of trapping time constants. One can view this as shifting the upper limit of the trapping time distribution to smaller values; i.e., deactivating the deeper traps that have long time constants. This interpretation is supported by Fig. 4, which compares the channel noise of the two MESFETs operating at 5 mA (ohmic regime) with two different gate voltages. The observed knee in the LTG-MESFET spectra is the upper limit of the trapping time constants. The 1/f part of the spectral intensity for the LTG-MESFET is slightly larger than

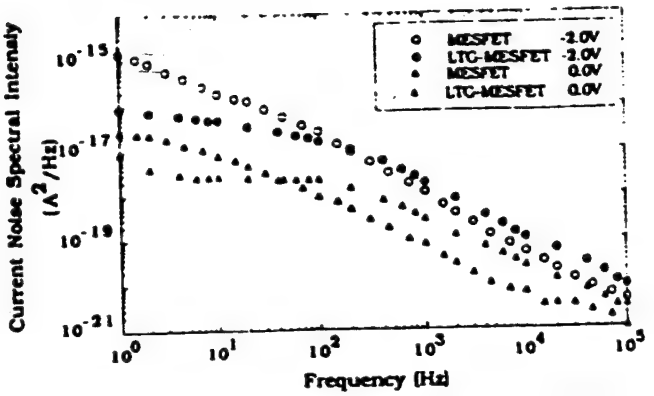

Fig. 4. Ohmic-regime noise spectra (I_{ds} = 5 mA) of the LTG-MESFET and MESFET for two different gate voltages.

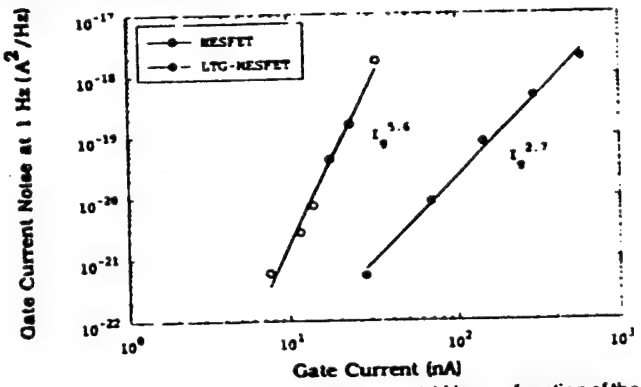

Fig. 5. Gate-current noise spectral intensity at 1 Hz as a function of the reverse gate current for both devices.

for the MESFET. (The spectra are measured in the ohmic regime at the same current so that comparison is warranted.) In addition, since the magnitude is a measure of the number of traps that are active, slightly more traps are active in the LTG-MESFET than in the MESFET. From these two observations, we conclude that for devices operating in the ohmic regime, the addition of the LTG passivating layer removes traps with larger activation energies and adds (only marginally) traps with smaller activation energies. Apparently, the modification of the surface changes the energy distribution of the traps. There have been examples where modification of the surface in MOSFETs reduced the trap density. In addition, experiments on buried channel MOSFETs and MESFETs showed improved noise performance.

GATE NOISE

To study the effect of gate current on noise, we measured the noise with the drain and source connected to ground and a reverse bias applied to the gate. Figure 5 shows the gate noise at 1 Hz as a function of the gate current with $V_{ds} = 0$ V. At a given gate current (10 nA < I_g < 1000 nA), the MESFET is much noisier and the current dependence of the noise is much stronger. For a given gate voltage, the LTG-MESFET has a larger gate current but a smaller noise coefficient, resulting in quieter operation than in the MESFET at an identical gate-voltage.

With this observation in mind, let us reexamine Fig. 4. We observe that the drain current noise of the MESFET increases more strongly as the gate voltage is changed from 0 to –2 V, at fixed drain current of 5 mA, than the noise of the LTG-MESFET. Changing the gate voltage from 0 to –2 V increases the gate current in both devices and increases the noise in the gate current of the MESFET more strongly (see Fig. 5). Since the gate current flows through the channel, the noise in the gate current does contribute to the drain current noise we measure, and could explain the larger increase of the MESFET drain current noise.

CONCLUSION

Including the LTG-GaAs layer as a passivating layer on top of the device seems to reduce the phase noise at low off-set frequencies. This is supported by measurements of the low-frequency noise. A noise reduction of 15 dB was observed when the MESFET and LTG-MESFET were biased in saturation with a drain current of 60 mA.

Further noise measurements taken when the devices were biased in the ohmic regime revealed that the passivation layer seems to deactivate the traps with larger activation energy and only marginally increase the density of the shallower traps.

The current dependence of the gate noise of the MESFET is much stronger than that of the LTG-MESFET and the noise level is larger for gate currents ranging from 10 to 1000 nA. As a result, for a given gate-to-source voltage, the MESFET is noisier than the LTG-MESFET. Further studies are underway to investigate a possible connection with the overlapping passivating layer.

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BREAKDOWN OF OVERLAPPING-GATE GaAs MESFET's

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Abstract

Gate-breakdown mechanisms in GaAs MESFET's have been studied by numerical simulation. The devices simulated include normal passivated and unpassivated MESFET's as well as overlapping-gate MESFET's passivated with low-temperature-grown (LTG) GaAs, normal GaAs, and silicon dioxide. The breakdown voltage is the highest for the overlapping-gate MESFET with LTG GaAs passivation, which agrees with the experimental results reported previously. The high breakdown voltage is the result of an altered electric field near the drain-edge of the Schottky-contact gate. This field modification is achieved most effectively by using an overlapping gate structure. The LTG GaAs is the best passivation layer because of its high resistivity and breakdown-field strength.

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I. Introduction

It has been shown that GaAs layers grown by molecular beam epitaxy (MBE) at low temperatures (~200 °C versus the normal ~600 °C) have very high resistivity and breakdown field strength. This low-temperature-grown (LTG) GaAs layer has been placed on top of the conducting GaAs layer of a MESFET to facilitate the formation of the overlapping-gate structure [1]. The gate breakdown voltage (~42 V) of this overlapping-gate MESFET is much higher than the 25 V for the MESFET without gate overlap. Although a Schottky contact is made directly to the conducting GaAs layer with the gate metallization, the measured breakdown voltage is nearly as high as that of a MISFET in which the entire gate is on a high-resistivity LTG GaAs layer [2,3]. Results from our many experiments consistently showed that the gate breakdown voltage is the highest for the MESFET with LTG GaAs passivation and an overlapping-gate structure, followed by the MESFET with LTG GaAs passivation without gate overlap, and the conventional MEFSET without passivation has the lowest breakdown voltage.

The purpose of this work is to better understand the mechanisms for the unusually high breakdown voltage of the overlapping-gate MESFET and to study how the gate structure and the properties of the passivation layer affect the breakdown voltage. Because of the uncertainty on the values of many physical parameters, such as the mobility, the saturation velocity, the impact ionization rate in various GaAs layers, and the density and energy level of the traps in the LTG GaAs, no attempt was made to match the calculated results with the experimental data. It is also not the intention of this work to simulate different type of the MESFET with its individual doping concentration and gate recess optimized for the highest breakdown voltage possible. All the MESFET's simulated here have the same dimensions and the properties of the conducting channel with differences only in the surface passivation and the gate structure. The values of the physical parameters used were chosen from previously published results to make the simulated results as realistic as possible.

II. Device Structures and Simulation Method

The cross-sectional structures of the MESFET's simulated are shown in Fig. 1. For normal MESFET's with and without surface passivation shown in Figs. 1(a) and 1(b), respectively, the gate length is 0.2 μm. For the overlapping-gate MESFET in Fig. 1(c), the length of the Schottky-contact portion of the gate on the conducting channel is 0.2 μm and the length of the overlap beyond the Schottky contact is 0.1 μm. For all the MESFET's the

gate is centered between a 1.4 μm source-drain spacing, and the n-type GaAs conducting channel is 500 Å thick and is doped to 6×10^{17} cm^{-3}. Undoped normal GaAs and LTG GaAs with different traps densities were used as the surface passivation layer on top of the conducting channel. An overlapping-gate MESFET with a silicon dioxide passivation layer was also simulated for comparison. The thickness of all the passivation layers is 200 Å.

The LTG GaAs has a very high resistivity (~ 10^7 Ω-cm) and a high breakdown field (~ 5×10^5 V/cm) [4]. A high density of point defects and precipitates caused by the excess As atoms in the LTG GaAs has been measured [5]. One of the two primary electrically active defects is a deep donor-like recombination center which is believed to be the As antisite defect As_{Ga} with its energy level near the middle of the band gap. The second one is an acceptor-like trap which is thought to be the gallium vacancy V_{Ga} with its energy level close to the valence band. The energy level and density of the traps depend strongly on the growth temperature and the subsequent annealing schedule. For growth temperatures between 200 and 300 °C, the densities for the donor and acceptor defects range from 10^{18} to 10^{19} and 10^{17} to 10^{18} cm^{-3}, respectively, after post-growth annealing. In the present simulation, relatively low densities of 5×10^{17} cm^{-3} for the acceptor and 1×10^{18} cm^{-3} for the donor were usually assumed for the LTG GaAs in order to provide rapid convergence of the numerical simulation. MESFET's with LTG GaAs having twice the trap densities were also simulated and showed only slight increase in the breakdown voltage. The donor defects were set at 0.7 eV below the conduction band while the acceptor defects were at 0.27 eV above the valence band [6].

The mobility of the electrons in the LTG GaAs with post-growth annealing is much lower than that of normal GaAs grown at a temperature near 580 °C. In this simulation the electron and hole mobilities used were 400 and 100 $cm^2/V \cdot s$ [6], respectively, for LTG GaAs, and 5000 and 400 $cm^2/V \cdot s$, respectively, for the normal GaAs. The experimental data for the saturation velocity of electrons in the LTG GaAs has not been reported. In this work, we assumed that the electron saturation velocity is 1×10^6 cm/s for LTG GaAs, which is one order of magnitude smaller than the 1×10^7 cm/s used for the normal GaAs. The uncertainty of the saturation velocity in the LTG GaAs could change the magnitude of the current and the breakdown voltage but should have little effect on the revelation of the breakdown mechanism. In normal GaAs layers the lifetime for electron and hole are assumed to be 1 and 20 ns, respectively. In LTG GaAs much shorter lifetimes of 0.1 ps for electrons and 2 ps for holes were used [4].

It has been shown that the surface depletion caused by surface traps in the GaAs has a profound effect on the breakdown voltage of a MESFET [7,8]. In this simulation, a single electron trap level at 0.7 eV below the conduction band edge with a density of 1 x 10^{12} cm^{-2} was assumed to be present at all normal GaAs surfaces. The occupancy of these traps varies with the bias conditions and the location of the traps in the MESFET in a manner similar to that reported in Ref. [7]. The same traps were assumed for the GaAs/SiO_2 interface also. Because of the high density of bulk deep levels already present, no surface traps were added to the LTG GaAs.

A commercially available two-dimensional device simulation program, BLAZE, was used for this study. It solves the Poisson's equation and the current continuity equations for both electrons and holes. The Shockley-Read-Hall recombination mechanism with fixed lifetimes is included. The generation rate due to the impact ionization is expressed as

$$G = \alpha_n n v_n + \alpha_p p v_p , \qquad (1)$$

where n and v_n are the concentration and velocity of electrons, and p and v_p are the concentration and velocity of holes. In Eq. (1) α_n and α_p are the ionization coefficients for electrons and holes with α defined as

$$\alpha = A \cdot \exp [- (B/E)^m], \qquad (2)$$

where E is the electric field component in the direction of the current flow. The constants used for both the normal GaAs and the LTG GaAs are A = 1.9 x 10^5 cm^{-1}, B = 5.75 x 10^5 V/cm, and m = 1.82 for electrons; and A = 2.22 x 10^5 cm^{-1}, B = 6.57 x 10^5 V/cm, and m = 1.75 for holes [9].

III. Simulation Results

The gate current of the MESFET was measured as a function of the drain voltage while biasing the gate at a constant -0.2 V. The gate breakdown voltage is defined as the voltage across the drain and the gate at which the reverse-biased gate current reaches 1 mA per millimeter of gate width. Table I lists the calculated breakdown voltages and other device parameters for various MESFET's. The normal MESFET without top GaAs passivation has the lowest breakdown voltage while the overlapping-gate MESFET with LTG GaAs passivation has the highest. The breakdown voltage of the normal MESFET

with LTG GaAs passivation falls in between the two. The calculations agree qualitatively with the experimental results [1]. Calculations show that use of an overlapping-gate structure over even a normal GaAs passivation layer (grown at ~580 °C by MBE) seems to increase the breakdown voltage also. However, a dielectric passivation layer appears less effective.

In Table I the drain saturation current $I_{d,sat}$, transconductance g_m, total gate capacitance C_g, and the output resistance R_{out}, all normalized to 1 mm gate width, were calculated at $V_{gs} = 0$ V and $V_{ds} = 4$ V. All MESFET's have approximately the same g_m and $I_{d,sat}$ except for the MESFET with oxide passivation which has a slightly higher current. As expected, the C_g is higher for the MESFET with the overlapping-gate structure, resulting in a lower unity-current-gain frequency f_T. The degradation of the f_T is approximately 10% for the overlapping-gate MESFET with LTG GaAs passivation. Because the overlapping portion of the gate shields the Schottky contact from the drain voltage, the output resistance of the overlapping-gate MESFET is much higher than that of a normal MESFET. A higher output resistance should increase the maximum oscillation frequency f_{max} and improve the efficiency for large-signal applications. Again, a dielectric passivation layer appears to provide less improvement.

A. MESFET's with and without gate overlap

Since it appears that the overlapping-gate structure is essential for the high breakdown voltage, we will first compare the simulation results of a normal planar MESFET without surface passivation (unpassivated MESFET), and MESFET's having an LTG GaAs passivation layer with (overlapping-gate MESFET) and without (LTG GaAs passivated MESFET) the 0.1 μm gate overlap.

For most GaAs MESFET's the breakdown occurs at the drain-side edge of the Schottky-contact gate, especially when the gate is negatively biased. It has been shown that the electric field near the gate can be reduced when the surface of the conducting channel between the gate and the drain is depleted [8,10]. Figure 2 shows the electron distribution in the three MESFET's biased at $V_{ds} = 6$ V and $V_{gs} = -0.2$ V. For the unpassivated MESFET, the surface depletion is caused by the electrons captured by the surface traps. The surface depletion width stays relatively constant from drain to gate till reaching the area very close to the gate edge where the depletion region caused by the Schottky-contact gate overlaps with that by the surface traps.

For the overlapping-gate MESFET, the depletion width at the surface of the conducting channel increases monotonically from the drain to the gate. The width starts to increase very rapidly near the edge of the overlapping gate which is 0.1 μm beyond the edge of the Schottky contact toward the drain. The overlapping portion of the gate acts like a secondary gate which originates an additional electric field. Because the overlapping gate is located above the conducting channel, this electric field has a large component perpendicular to the surface of the channel and therefore can effectively modulate the depletion width. This is equivalent to varying the surface trap density along the conducting channel with an increasing density near the Schottky gate. This artificially varied surface trap density results in an optimal field distribution because a large surface depletion near the gate favors a high breakdown voltage while a small depletion away from the gate would maintain a low drain resistance.

Figure 3 shows the contour plots of the electric field for the three MESFET's. It is clearly seen that for the unpassivated MESFET the highest electric field in the channel is at the drain-edge of the Schottky gate. On the other hand, for the overlapping-gate MESFET the maximum field is in the LTG GaAs passivation layer directly under the edge of the overlapping portion of the gate. For the passivated MESFET the maximum electric field is still in the conducting channel near the edge of the Schottky-contact gate, but the magnitude of the field is smaller than that of the unpassivated MESFET.

The magnitude of the electric field near the surface of the conducting channel between the source and the drain contacts is shown in Fig. 4. In the overlapping-gate MESFET the electric field peaks at the point directly under the edge of the overlapping portion of the gate, and a secondary peak occurs at the Schottky gate. Because of the two electric-field peaks, the field near the gate spreads out over a large distance and the magnitude of the field decreases. The electric field peak near the drain ohmic contact observed by other studies [7,8] was not evident in our simulation because of the high doping concentration in the channel of the present MESFET's. The field starts to increase at the edge of the drain contact when this doping concentration falls below 2×10^{17} cm^{-3}.

As expected from the field distribution result, the impact generation rate is the highest at the drain side of the gate in the unpassivated MESFET. In the LTG GaAs passivated MESFET the generation rate at the same location is approximately two orders of magnitude smaller. For the overlapping-gate MESFET the highest impact generation rate is found in the LTG GaAs passivation layer under the overlapping portion of the gate, and the rate is another order of magnitude smaller than that in the passivated MESFET. For

approximately the same field strength, the generation rate in the LTG GaAs is much smaller than that in the normal GaAs. In the LTG GaAs fewer available carriers due to shorter lifetimes in conjunction with lower carrier mobilities would suppress the impact generation rate expressed in Eq. (1).

B. MESFET's with and without LTG GaAs passivation

In this section the simulated results of MESFET's (no gate overlap) with and without LTG GaAs passivation will be compared. In Fig. 5, paths are plotted along the direction of the electric field from locations on the constant electron concentration contour in the channel to the gate. The same plot for the overlapping-gate MESFET is also shown for comparison. For the MESFET with LTG GaAs passivation the traces from points in the channel pass through the passivation layer to the gate. For the unpassivated MESFET most traces are nearly parallel to the surface of the channel and always close to the surface because of the small vertical component of the electric field.

Since along the traces shown in Fig. 5 the electric field E is parallel to the incremental path length $d\ell$, the total voltage drop $\int \mathbf{E}\cdot d\boldsymbol{\ell}$ is proportional to the product of the field strength and the path length. For the same voltage difference between the gate and a given point at the boundary of the depletion region in the channel (where the electric field approaches zero), a smaller average E field requires a longer path. Comparing Figs. 5 and 3, it is apparent that the average field strength along the traces in the unpassivated MESFET is much higher than that in the passivated MESFET. A longer path in the passivated MESFET means a wider depletion region at the top of the conducting channel. As a result the undepleted conducting channel thickness starts to decrease at location further away from the drain-edge of the gate. To maintain a constant current throughout the channel, the rate of increase for electric field parallel to the surface of the channel intensifies when the thickness of the conducting channel starts to shrink. Therefore, the drain-voltage drops along the channel more quickly and also starting further away from the drain side of the gate. Consequently, the voltage difference between the gate and the channel near the gate becomes smaller resulting in a lower electric field at the gate.

Also notice that in the unpassivated MESFET most traces terminate close to the edge of the gate. On the other hand, the traces in the passivated MESFET are more widely spread over the gate, and the field lines are less crowded at the edge of the gate. This is another reason that the breakdown voltage of the passivated MESFET is higher. For the

overlapping-gate MESFET a large percentage of the traces terminate at the overlap portion of the gate, resulting in a further reduction of the density of the field lines on the Schottky gate. The starting point of the increasing surface depletion in the channel is furthest away from the drain-edge of the Schottky gate of any MESFET, because of the extension of the overlap toward the drain and its position above the conducting channel.

C. Overlapping-gate MESFET's with normal and LTG GaAs passivation

In this section we examine the effect of different types of GaAs passivation on the breakdown voltage of the overlapping-gate MESFET. When a normal undoped GaAs layer was used as the surface passivation, it was assumed that there are no interface traps between the undoped passivation layer and the n-type conducting channel because all the layers are grown in situ. However, the same 1×10^{12} cm^{-2} surface states were assumed present at the top surface of the GaAs passivation layer.

The electric fields along the top surface of the conducting channel from the source to the drain of the MESFET's with LTG GaAs and normal GaAs passivation are plotted in Fig. 6. The electric field peaks under the drain-edge of the overlapping portion of the gate. The magnitude of the maximum field increases with decreasing traps in the passivation layer and is the highest for the normal undoped GaAs. However, the difference of this maximum field is relatively small. Notice that the magnitude of the electric field outside the gate area is higher for LTG GaAs passivation. This is because the LTG GaAs passivation layer with high trap densities causes a larger depletion region at the surface of the conducting channel resulting in a higher electric field in the channel. The highest impact ionization rate is always in the passivation layer directly under the drain-edge of the overlapping gate with a lower rate in the conducting channel near the gate.

D. Overlapping-gate MESFET with oxide passivation

Since SiO_2 has been widely used as the surface passivation for GaAs MESFET's, it is interesting to examine whether using this oxide in the overlapping-gate structure can also improve the breakdown voltage. It was assumed that the same trap density of 1×10^{12} cm^{-2} is present at the interface of the conducting channel and the oxide passivation layer and there are no bulk traps in the oxide. Because the oxide is an insulator and is free of traps, the electric field in the oxide is nearly constant as shown in the contour plot of Fig. 7. Since the dielectric constant of the oxide is approximately one third of that for GaAs and most interface traps are empty because of the negative bias on the gate, the electric field in the oxide is much higher than that in the conducting channel and the field drops sharply

across the interface from the oxide to the GaAs channel. As a result the overlapping portion of the gate is not very effective in depleting the electrons in the channel, which is the requirement for reducing the field strength at the Schottky contact. This is demonstrated by the plot of the electric field near the top of the channel, shown in Fig. 6. Although the electric field in the channel does increase under the drain-edge of the overlapping portion of the gate, the overlapping gate is not effective enough to shift the maximum field away from the edge of the Schottky contact. The highest impact generation rate is still found in the area near the drain-edge of the Schottky contact.

IV. Summary

The simulation results show that the overlapping-gate MESFET with LTG GaAs passivation has the highest breakdown voltage and the LTG GaAs passivated MESFET without gate overlap has a breakdown voltage higher than that of an unpassivated MESFET. The result agrees with the experimental data reported previously. The essence of achieving a high breakdown voltage in a GaAs MESFET is to have an increasing depletion width at the surface of the conducting channel from the drain to the Schottky gate. However, this width increase cannot be caused by the electric field originating directly from the drain-edge of the Schottky gate because this will not reduce the electric field at the edge of the gate.

In an overlapping-gate MESFET, the electric field originating from the overlapping portion of the gate contributes to the formation of the depletion region in the passivation and conducting channel layers between the gate and the drain. This is equivalent to providing additional trapped charge at the surface of the conducting channel, resulting in a lower electric field at the drain-edge of the Schottky contact. Since the most critical requirement is to widen the depletion region near the drain-edge of the Schottky contact, the length of gate overlap does not have to be large. Because the breakdown takes place in the passivation layer, it is plausible that the breakdown voltage of the overlapping gate MESFET is comparable to that of a MISFET with the same passivation layer as the gate insulator.

The breakdown voltage increases with the presence of an LTG GaAs passivation layer even without gate overlap. Part of the electric field associated with the charge on the Schottky gate is confined to the passivation layer and terminates at the ionized dopants in the channel, resulting in a wider depletion region. However, the depletion-width widening is not as substantial as that by the overlapping gate. Consequently, the breakdown-voltage

increase is smaller. The thickness of the passivation layer needed to increase the breakdown voltage depends on the dimension and other physical parameters, such as the doping concentration of the channel. Usually, this passivation layer does not have to be very thick but it must have a high resistivity and should have a dielectric constant similar to that of the channel material. Because of the low dielectric constant and the high density of interface traps, a deposited dielectric passivation layer for the overlapping-gate structure is less effective to improve the breakdown voltage.

In conclusion, the simulation in this work explains the mechanism of increasing breakdown voltage of a GaAs MESFET with the addition of a passivation layer. The breakdown voltage can be further improved by the combination of a proper passivation layer and an overlapping-gate structure. Because of the high resistivity and high breakdown strength, the GaAs grown in-situ at low temperatures appears to be the best passivation layer. For large-signal operations the benefits of increased breakdown voltage and the output resistance of an overlapping-gate MESFET with LTG GaAs passivation outweigh the relatively small increase of the gate capacitance.

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Figure Captions

Fig. 1 Structure of the MESFET's simulated. (a) Normal unpassivated MESFET. (b) Normal passivated MESFET. (c) Overlapping-gate MESFET. The passivation layer can be normal GaAs, LTG GaAs, or oxide. The Schottky-contact gate is the portion of the gate metallization in contact with the conducting channel.

Fig. 2 Electron concentration in MESFET's biased at V_{gs} = -0.2 V and V_{ds} = 6 V. (a) Normal unpassivated MESFET. (b) Normal LTG GaAs passivated MESFET. (c) Overlapping-gate MESFET with LTG GaAs passivation. S indicates source, G gate, and D drain.

Fig. 3 Electric field in the same MESFET's shown in Fig. 2.

Fig. 4 Magnitude of the electric field near the surface of the conducting channel.

Fig. 5 Electric field and electron concentration in the MESFET. The electric-field traces originate at the boundary of the depletion region with electron concentration of 1 x 10^{16} cm^{-3} and follow the direction of the field. (a) Normal unpassivated MESFET. (b) Normal LTG GaAs passivated MESFET. (c) Overlapping-gate MESFET with LTG GaAs passivation.

Fig. 6 Magnitude of the electric field near the top of the conducting channel for overlapping-gate MESFET's with different passivation layers.

Fig. 7 Electric field in the overlapping-gate MESFET with oxide passivation.

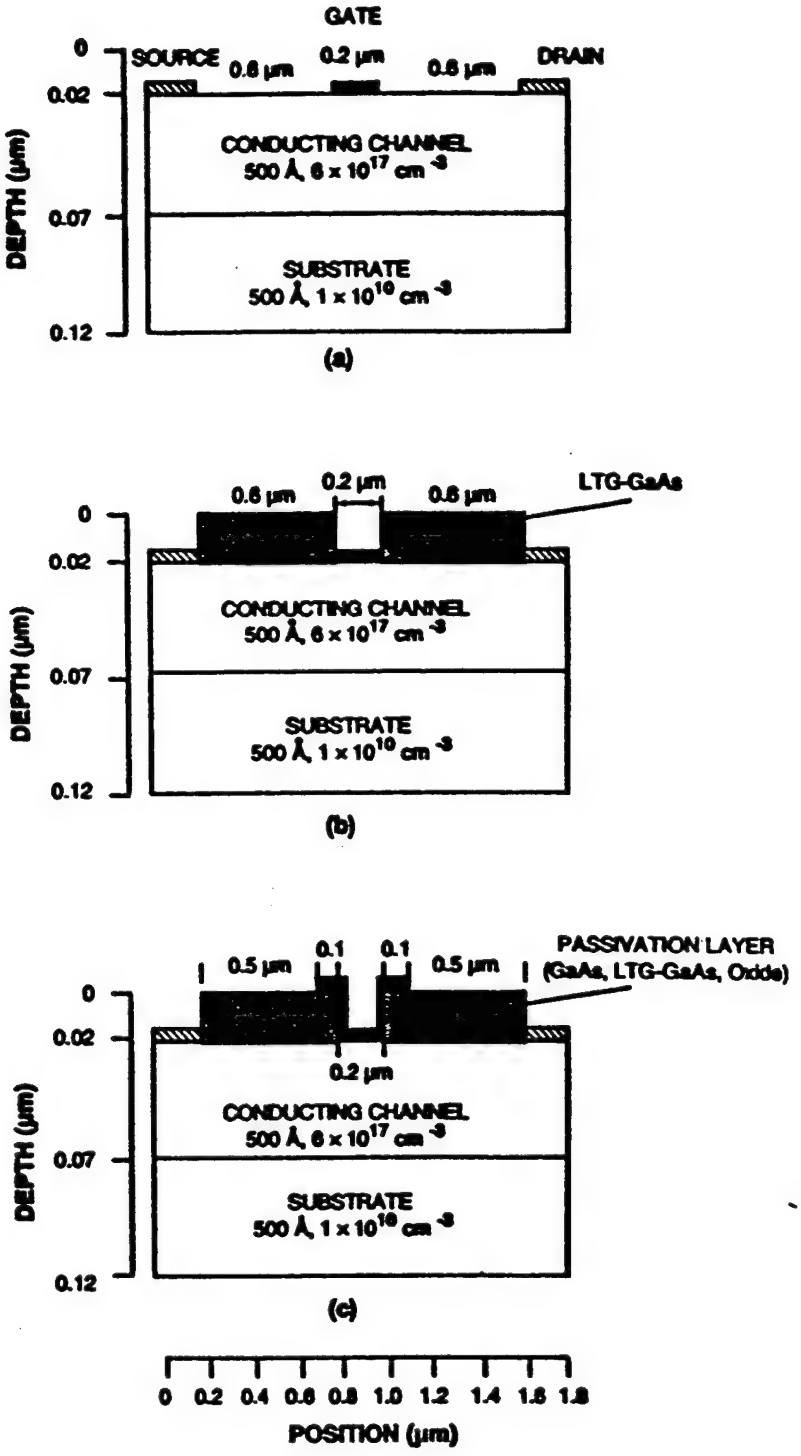
GATE
SOURCE
DRAIN
0.6 μm
0.2 μm
0.6 μm
0
0.02
0.07
0.12
DEPTH (μm)
CONDUCTING CHANNEL
500 Å, 6 x 10^17 cm^-3
SUBSTRATE
500 Å, 1 x 10^10 cm^-3
(a)
LTG-GaAs
(b)
PASSIVATION LAYER
(GaAs, LTG-GaAs, Oxide)
0.5 μm
0.1
0.1
0.5 μm
0.2 μm
(c)
0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8
POSITION (μm)
254298-1

Fig. 1

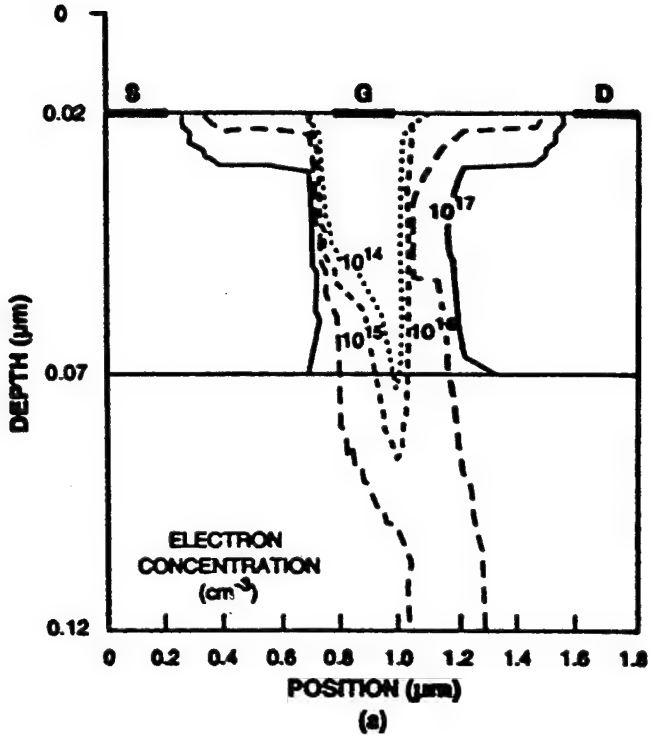

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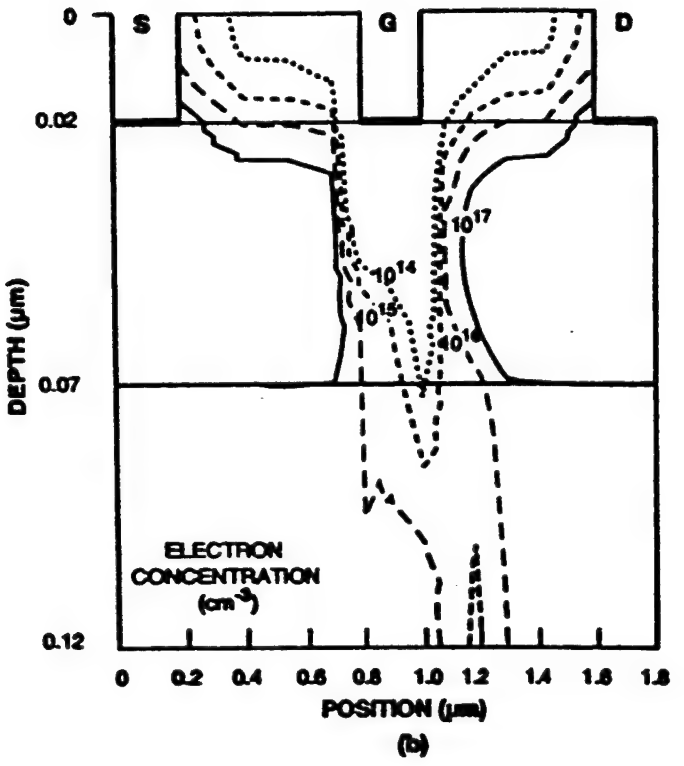
Fig. 2(a)



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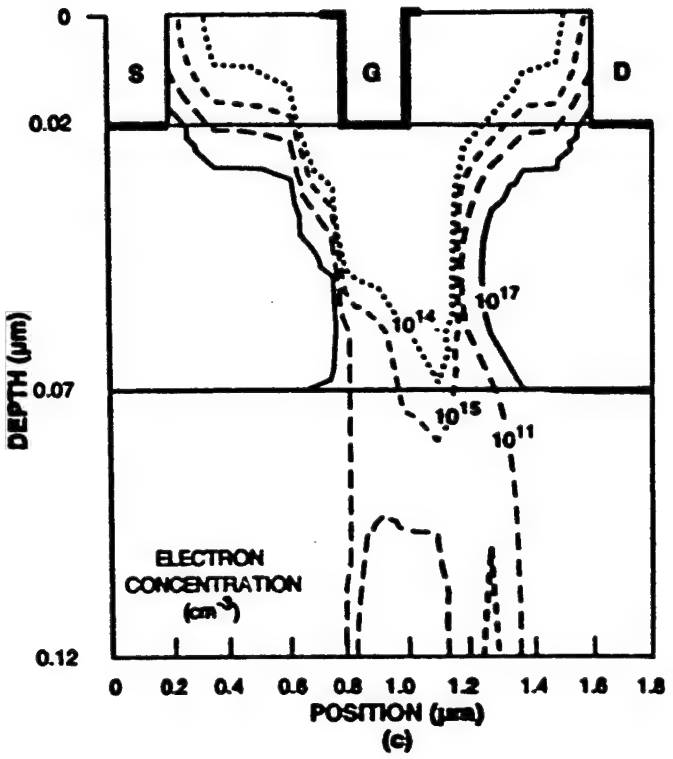
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ELECTRON CONCENTRATION (cm^{-3})
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0.2
0.4
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1.8
POSITION (μm)
(c)
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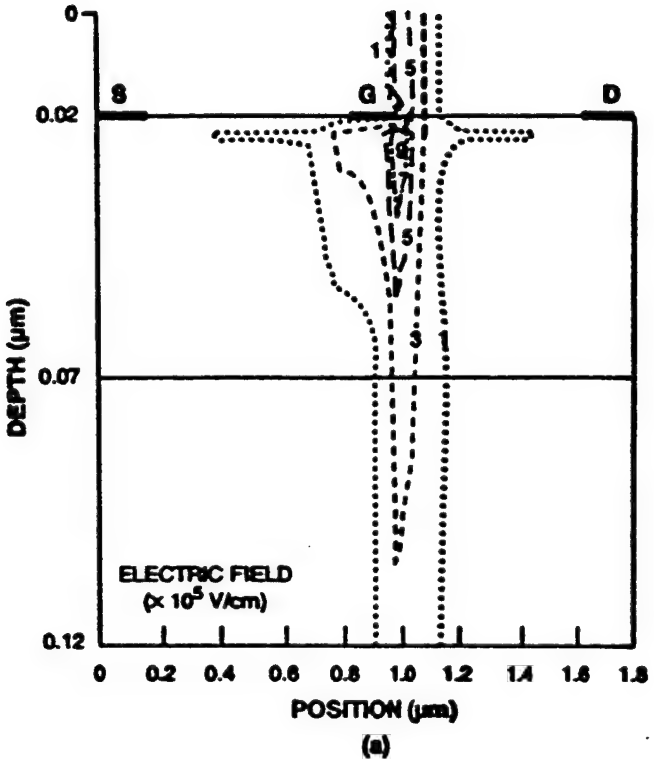
Fig. 2(c)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(a)
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Fig. 3(a)

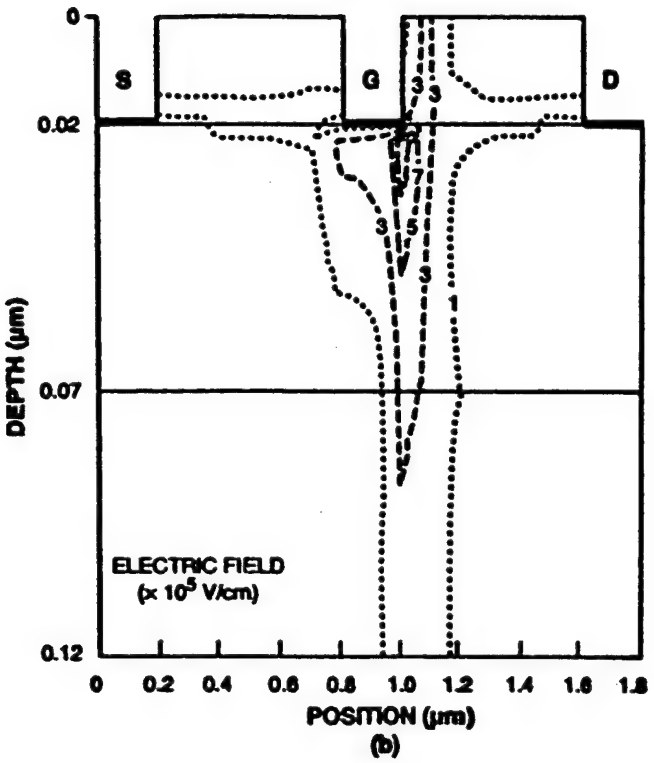
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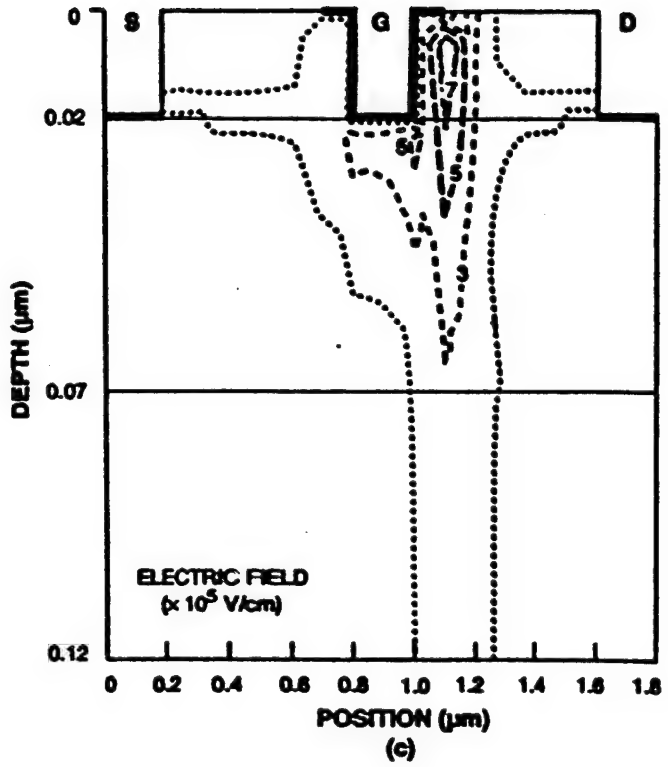
Fig. 3(b)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D
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0.02
0.07
0.12
DEPTH (μm)
ELECTRIC FIELD
(x 10^5 V/cm)
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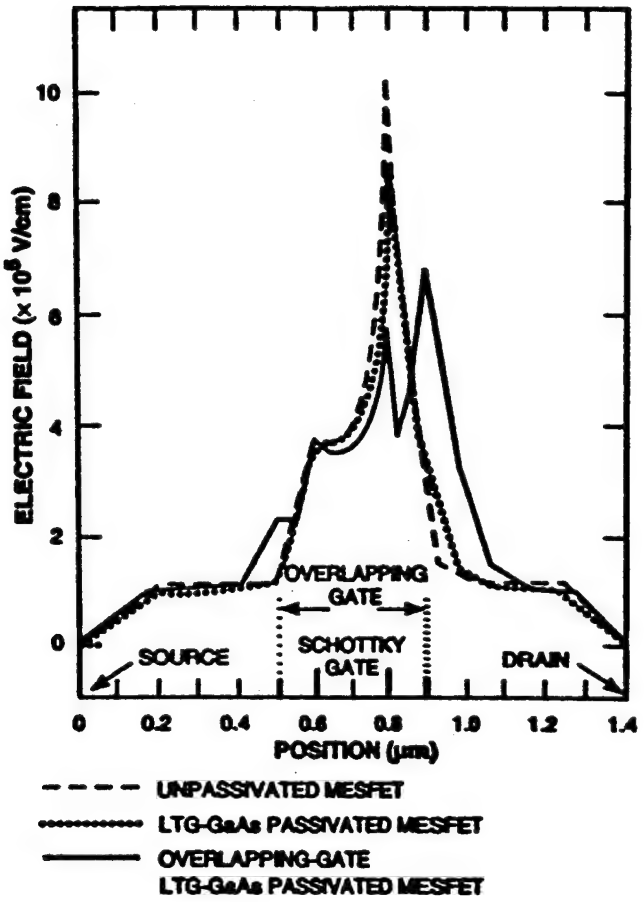
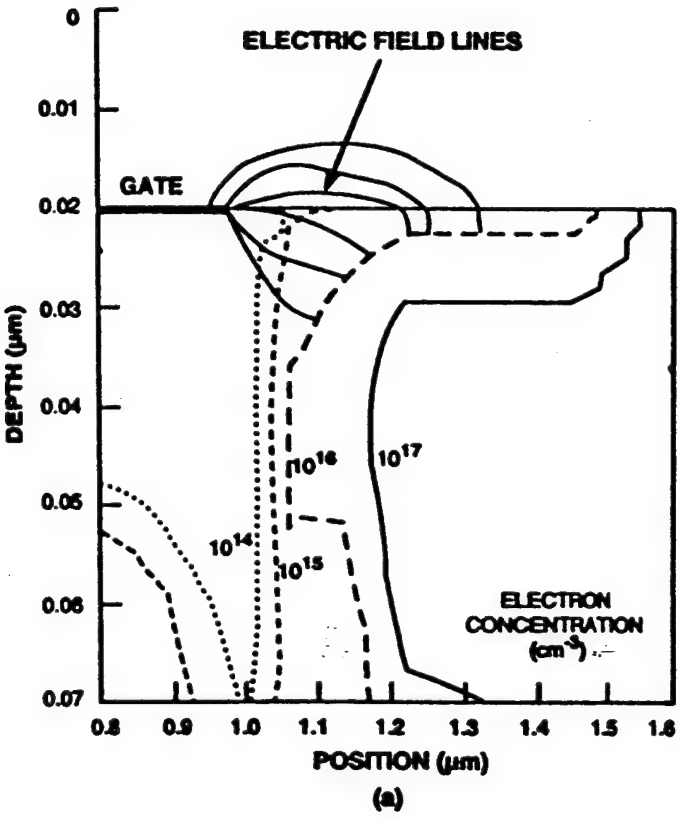
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
POSITION (μm)
(c)

Fig. 3(c)



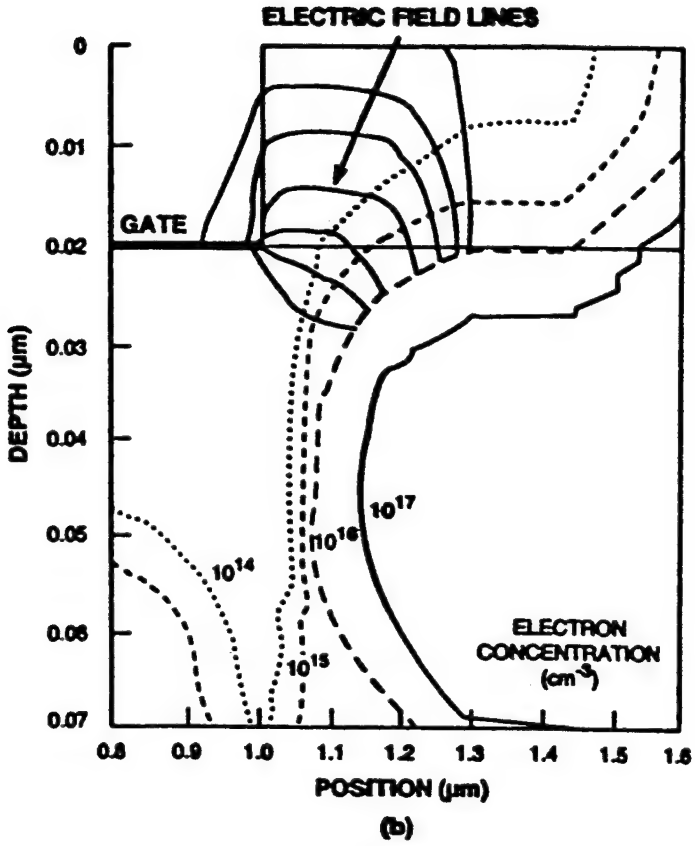
343648-8

Fig. 4



343886-1

Fig. 5(a) --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DEPTH (μm)
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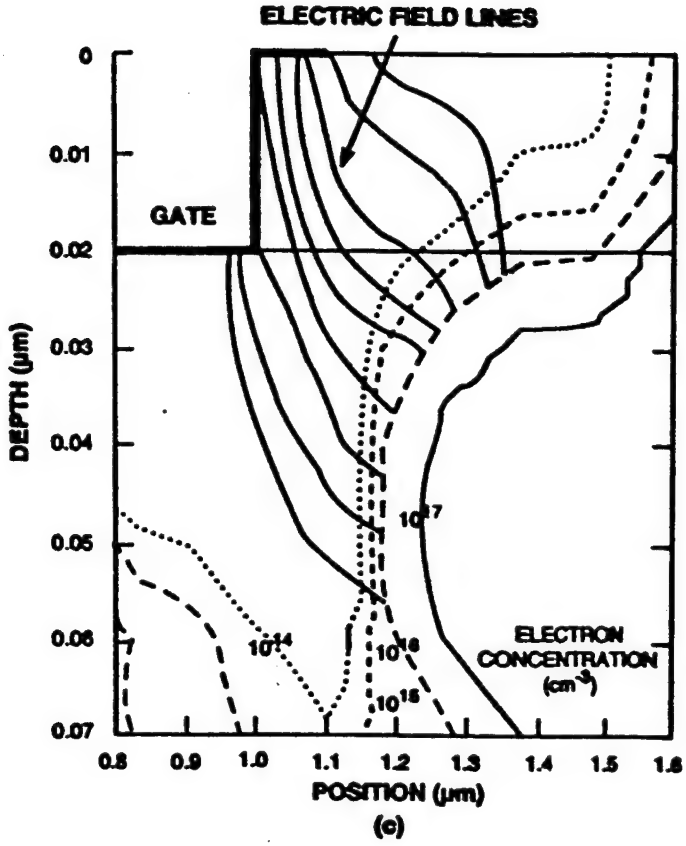
0.03
0.04
0.05
0.06
0.07
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
1.6
POSITION (μm)
10^{14}
10^{15}
10^{16}
10^{17}
ELECTRON CONCENTRATION (cm^{-3})
(b)
243464-3

Fig. 5(b)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GATE
DEPTH (μm)
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0.02
0.03
0.04
0.05
0.06
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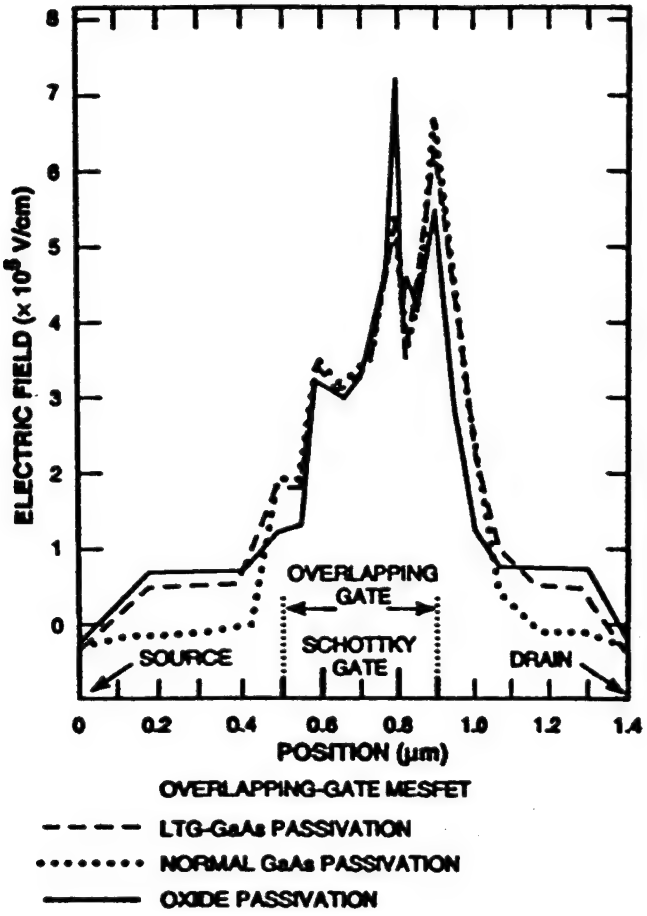
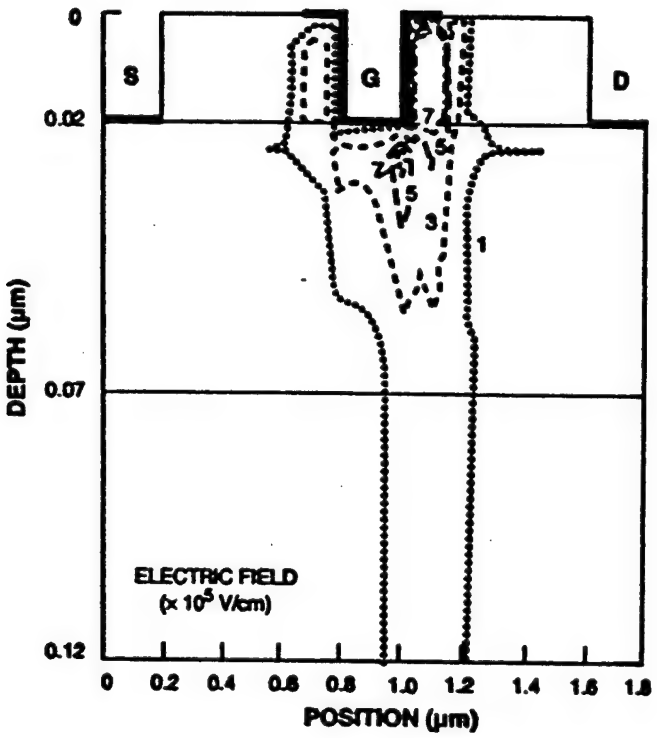
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
1.6
POSITION (μm)
10^{17}
10^{14}
10^{16}
10^{15}
ELECTRON CONCENTRATION (cm^{-3})
(c)

Fig. 5(c)



243484-1

Fig. 6



243464-16

Fig. 7

Table I
Calculated Parameters of MESFETs

MESFET Type	Breakdown Voltage (V)	$I_{d,sat}$ (mA)	g_m (mS)	C_g (pF)	R_{out} (Ω)	f_T (GHz)
Normal, unpassivated	7.6	39.7	178	.64	482	44.3
Normal, LTG GaAs passivated	8.7	38.7	179	.66	634	44.2
Overlapping gate, normal GaAs passivated	9.4	37.7	176	1.07	1137	26.3
Overlapping gate, LTG GaAs passivated	10.9	37.6	176	.70	1086	39.8
Overlapping gate, oxide passivated	8.6	42.9	176	.82	446	34.1

SELF-ALIGNED GaAs MISFET's WITH A LOW-TEMPERATURE-GROWN GaAs GATE INSULATOR

C. L. Chen, L. J. Mahoney, K. B. Nichols, M. J. Manfra, B. F. Gramstorff, K. M. Molvar, R. A. Murphy, and E. R. Brown

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Abstract

GaAs MISFET's with a low-temperature-grown (LTG) GaAs gate insulator and ion-implanted self-aligned source and drain n^+ regions are demonstrated. The resistivity and breakdown field of the LTG GaAs insulator were not changed appreciably by implantation and 800°C activation annealing. The gate leakage current remained very low, at a value of approximately 1 μA per μm^2 of gate area at 3 V forward gate bias. Because of the reduced source and drain resistance, the drain saturation current and the transconductance of self-aligned MISFET's increased more than twofold after ion implantation .

This work was supported by the Department of the Air Force, in part by a program with the Air Force Office of Scientific Research.

channel were chemically etched using the W gate metallization as the etch mask. Citric acid and HCl were used to selectively etch the GaAs and AlAs, respectively. Next, the source and drain regions were implanted with Si using one of the implant schedules. In one schedule (sample A), the energy was 30 keV and the total dose was 2×10^{13} cm^{-2}. For the other schedule (sample B), the energy was 50 keV and the total dose was 3×10^{13} cm^{-2}. The implanted samples were thermally annealed at 800 °C for 10 s. Next, standard Ni/Ge/Au source and drain ohmic contacts were defined by liftoff and alloyed. The spacing between the source and drain ohmic contacts was approximately 7 μm. Finally, the devices were isolated by proton implantation. For comparison, a control sample that was neither implanted nor annealed was also processed on the same material in parallel with the self-aligned MISFET.

III. Experimental Results

The sheet resistance of the conducting channel outside the gate area was 1700 Ω/square without Si implantation, and was reduced by the implant to 620 Ω/square for sample A and 480 Ω/square for sample B. The contact resistance was also improved from 6.6×10^{-6} Ω cm^2 for the control sample to 1.1×10^{-6} Ω cm^2 for sample A and 5.4×10^{-7} Ω cm^2 for sample B.

The I-V characteristics of the MISFET's are shown in Fig. 2. The maximum drain current obtainable was 65 mA/mm (V_{gs} = +2 V) for the control sample, 160 mA/mm (V_{gs} = +4 V) for sample A, and 200 mA/mm (V_{gs} = +6 V) for sample B. The corresponding pinch-off voltages are -1.5 V for the control, -1.8 V for sample A, and -3.0 V for sample B. The maximum g_m also increased from approximately 20 mS/mm for the control to 35 and 45 mS/mm on samples A and B, respectively. Notice that even at 6 V of forward gate bias, there is no sign of gate conduction. The cause for the apparent g_m compression shown in Fig. 2(c) is not fully understood. It may be related to Fermi-level pinning due to traps in the LTG GaAs insulator.

The forward-biased gate current of the MISFET's is plotted in Fig. 3. The gate current of self-aligned MISFET's is higher than that of the control MISFET and it appears to increase with implant energy and dose. At a forward gate current of 10 nA per μm^2 gate area, which is acceptable for many applications in low-power digital circuits, the corresponding positive voltages on the gate are 1.83, 1.56, and 1.08 V for the MISFET's on the control sample, sample A, and sample B, respectively. The reverse gate-breakdown

voltage, also defined at 10 nA per μm^2 gate area, is 18 V for sample B and above 20 V for sample A and the control sample.

RF measurements were performed using microwave on-wafer probes. The unity-current-gain frequency f_T, derived from measured small-signal scattering parameters, is 2.2, 5.7, and 7.4 GHz for the MISFET's on the control sample, sample A, and sample B, respectively. The drain bias was kept at 2 V, and gate biases, chosen for a high g_m, were -0.5, 0, and -1.5 V, respectively. The corresponding values of the maximum frequency of oscillation f_{max} are 1.6, 2.9, and 4.1 GHz, respectively. The low f_{max} values are probably caused by the high resistance of the thin W gate. Because of the MIS structure, the estimated 0.1 pF of gate capacitance for sample A at 0 V gate voltage was approximately 50% lower than that of a MESFET with the same doping concentration.

IV. Discussion and Summary

Self-aligned GaAs MISFET's with an LTG GaAs gate insulator have been demonstrated. The performance improvement caused by the n^+ implantation is clearly shown. The self-aligned MISFET's have a low gate-leakage current and f_T values comparable to those of GaAs MESFET's with similar physical device parameters indicating that the high-temperature annealing did not produce any severe adverse effect. Large gate dimensions and a lightly doped channel were used in this experiment in order to easily identify the effects of the n^+ implantation, which by itself was not optimized in the current process. Therefore, the modest characteristics of the MISFET's were expected and should by no means be considered as the performance limit of the self-aligned LTG GaAs MISFET. In order to increase the speed of the MISFET, the thickness of the LTG GaAs insulator and the gate length should be reduced and the implant and annealing schedules should also be optimized. Experiments in these areas are currently in progress.

The success of this work opens the door to a new class of GaAs MISFET with the potential of being the ideal device for low-power and high-speed applications. The fabrication process is simple and is standard for GaAs IC's. Because there is no gate recess, the threshold voltage is determined mainly by the epitaxial growth, and good device uniformity can be expected.

Acknowledgments

The authors would like to thank R. F. Murphy, C. T. Harris, and G. D. Johnson for their technical support, R. Actis and R. G. Drangmeister for RF measurements, and J.

D. Woodhouse as well as J. K. Abrokwah and V. Nair of Motorola for many helpful discussions.

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Figure Captions

Fig. 1 Layer structures and process steps for the self-aligned LTG GaAs MISFET.

Fig. 2 I_{ds} versus V_{ds} characteristics of MISFET's with 100-μm-wide gate width. (a) Control MISFET. The vertical scale is 1 mA/div and V_{gs} is +2 V for the top curve with 1-V steps. (b) Self-aligned MISFET with 30 keV implant. The vertical step is 2 mA/div and V_{gs} is +4 V for the top curve with 2-V steps. (c) Self-aligned MISFET with 50 keV implant. The vertical step is 2 mA/div and V_{gs} is +6 V for the top curve with 2-V steps. The horizontal scale is 500 mV/ div for all the I-V curves

Fig. 3 Measured forward-biased gate current of the 100-μm-wide control and self-aligned MISFET's.

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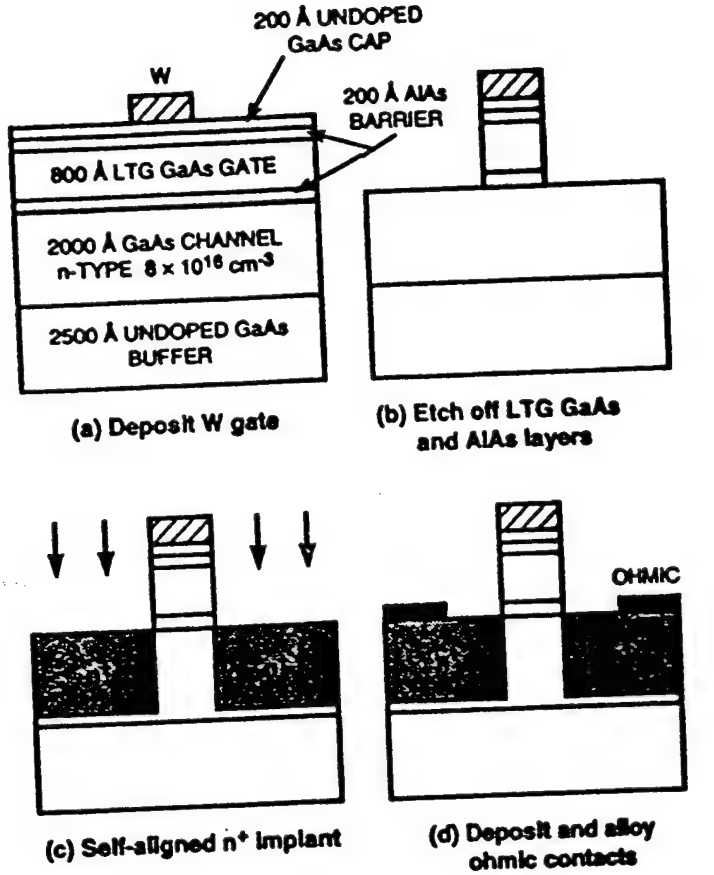

200 Å UNDOPED
GaAs CAP
W
200 Å AlAs
BARRIER
800 Å LTG GaAs GATE
2000 Å GaAs CHANNEL
n-TYPE 8 x 10^18 cm^-3
2500 Å UNDOPED GaAs
BUFFER
(a) Deposit W gate
(b) Etch off LTG GaAs
and AlAs layers
OHMIC
(c) Self-aligned n+ implant
(d) Deposit and alloy
ohmic contacts
245662-3

Fig. 1

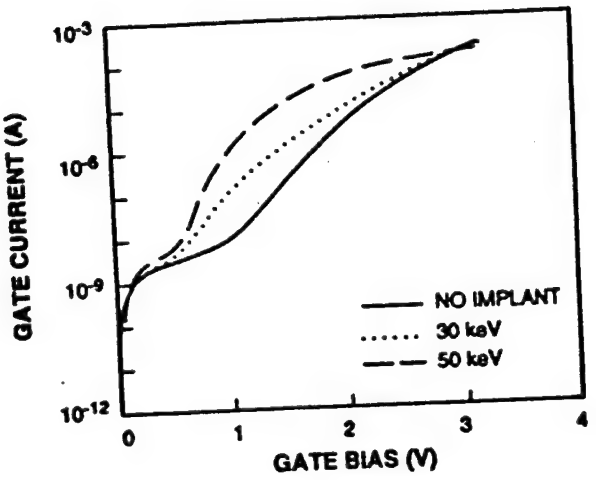
(a)

(b)

(c)

245662-4L

Fig. 2



248263-1

Fig. 3

EFFECTS OF THE LOW-TEMPERATURE-GROWN GaAs AND AlGaAs ON THE CURRENT OF AN MIS STRUCTURE

C. L. Chen, L. J. Mahoney, K. B. Nichols, M. J. Manfra, E. R. Brown, P. M. Nitishin, K. M. Molvar, B. F. Gramstorff, and R. A. Murphy

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Abstract

GaAs and AlGaAs layers grown by molecular beam epitaxy at low temperatures were used as the insulator in a metal-insulator-semiconductor (MIS) diode simulating the gate structure of a GaAs MISFET. The diode current increases after the high-temperature annealing at 800 °C for 10 s, a schedule commonly used for ion-implantation activation, and the amount of the increase depends strongly on the insulator material and the growth temperature. It appears that the LTG GaAs grown at 200 °C and the LTG $Al_{.43}Ga_{.57}As$ grown at 300 °C, both embedded between AlAs barrier layers grown at a normal temperature, are the two best gate insulators when the high-temperature annealing is a required process for the MISFET. For a diode with a 300-Å-thick $Al_{.43}Ga_{.57}As$ insulator and 100-Å-thick AlAs barriers, 1.42 V forward bias results in a leakage current of 1 nA per μm^2 diode area. This low diode current proves that the LTG insulator is suitable for the gate of MISFETs.

I. Introduction

GaAs and AlGaAs layers grown by molecular beam epitaxy (MBE) at low temperatures (usually below 300 °C) have a very high resistivity and breakdown field. Used as the buffer layer for MESFETs, the low-temperature grown (LTG) layer reduces the sidegating and short-channel effects [1]. LTG GaAs has also been successfully used as the gate insulator of GaAs metal-insulator-semiconductor field-effect-transistors (MISFETs) to increase the breakdown voltage and the output power [2,3]. The same LTG-GaAs MISFETs are ideal for low-voltage and low-power applications because the gate can be forward biased without drawing significant gate current and can be easily biased with a single power supply. Forward-bias gate leakage current is a very important device parameter in low-power electronics because it determines the stand-by power consumption and affects the logic levels and the noise margin.

Recently, we demonstrated LTG-GaAs MISFETs with significantly lowered knee voltage and increased transconductance g_m because of self-aligned n^+ implantation in the source and the drain regions [4]. Since the LTG GaAs is known to lose its high resistivity during the high-temperature annealing required for implant activation [5], the MIS layer structures previously used for the gate insulator had to be modified to minimize the degradation. The purpose of this work is to investigate the effect of post-implant annealing on the gate leakage current for various LTG GaAs and AlGaAs layers and to determine the optimal gate structure for self-aligned MISFETs. The LTG AlGaAs was also included in this study because the LTG AlGaAs has been shown to have a resistivity even higher than the LTG GaAs [6,7] suggesting that LTG AlGaAs could be a better gate insulator. In order to simplify the measurement, in this work MIS diodes with layer structures used for the gate insulator of MISFETs were used to simulate the behavior of the gate.

II. Background and Experiment Design

Although the theory for carrier transport in LTG GaAs is still not well established [8], it is generally believed that the high resistivity is related to As precipitates and deep traps found in the LTG GaAs. The density of the deep trap and the effective volume of the As precipitate decreases after the annealing in the temperature range for implant activation, resulting in a reduction of the resistivity. Furthermore, the As precipitates can be lost

during the high-temperature annealing by outdiffusing to the surface and evaporate from the wafer [9]. This excess-As loss can occur even during the more modest 600 °C post-growth in-situ annealing in the MBE chamber [10], and the loss is more severe during the implant activation annealing which is usually done at temperatures above 800 °C. Any loss of As precipitates can be serious for the MISFET because only a thin LTG insulator is used for the gate and, thus, the number of the As precipitates is limited. Because it has been shown that an AlAs layer is a good diffusion barrier for As precipitates in quantum-well structures [11,12], such a layer is added to the top of the LTG insulator in our MIS structure to prevent As outdiffusion during the high temperature annealing. The addition of this top AlAs barrier is the major departure from the standard MIS gate structure used in previous work [2,3].

The parameters associated with the insulator that affect the current are the growth temperature, layer thickness, and the type of the insulator, such as whether it is a GaAs or AlGaAs and the Al mole fraction in the AlGaAs. Since the density of the deep traps and the As precipitates in the LTG GaAs generally increase with decreasing growth temperatures to approximately 200 °C [8,13,14], the resistivity also increases with decreasing growth temperature. Intuitively, a low growth temperature should be used for a high-resistivity gate. However, the traps and the As precipitates are very sensitive to the high-temperature annealing, it is expected that the properties of the LTG GaAs grown at lower temperature would be affected more by the annealing. Therefore, one of the goals of this work is to determine whether a low-growth-temperature is still preferred when the layer will be subjected to implant-activation annealing. In this experiment, LTG GaAs layers were grown at either 200 °C or 350 °C and the LTG AlGaAs layers were grown at 250 °C or 300 °C to investigate the effect of the growth temperature. Because AlGaAs grown at the normal temperature has been used as the gate material to reduce the gate current with some success [15], the AlGaAs layer grown at the normal 600 °C was also compared.

The diode current always decreases with increasing insulator thickness, but in order to maintain a high g_m the gate insulator should be kept as thin as possible so long as the gate current is acceptably low. In this work, diodes with 300- and 800-Å-thick insulators are studied. When the diameter of the As precipitate becomes comparable to or greater than the thickness of the LTG GaAs, the precipitates have a tendency to diffuse through thin AlGaAs or AlAs barriers to the neighboring layers [12]. As a result, the resistivity of the LTG GaAs can decrease dramatically and the outdiffused As may destroy the adjacent conducting channel. Even if the LTG GaAs layer can accommodate all the precipitates, a high density of As precipitates in a thin layer may form a continuous semi-metallic sheet

and prevent channel modulation [12]. Therefore, the LTG AlGaAs, which has a far lower density of As precipitates and slower growth rate of the size of the As precipitate, seems more suitable for thin-insulator applications than the LTG GaAs. Because of these considerations, in our study only AlGaAs layers were used for the thin 300-Å insulator while both GaAs and AlGaAs layers were compared as the 800-Å insulator. In addition, among diodes with a 300-Å-thick insulator, LTG AlGaAs layers with 31% and 43% Al mole fractions are compared to investigate the effect of the bandgap on the resistivity.

The experimental results in this report are divided into three parts. In the first part, an LTG GaAs MISFET structure was examined by the transmission electron microscopy (TEM). In the second part of the experiment, the effect of the implant-activation annealing on the diode current of MIS structures with 800-Å-thick LTG GaAs or LTG $Al_{.31}Ga_{.69}As$ insulator was studied. In the final part, the insulator was limited to the 300-Å-thick AlGaAs. The effects of varying the Al mole fraction of the AlGaAs and the growth temperature are included in this section.

III. Device Fabrication

As shown in Fig. 1, the MBE-grown epitaxial layers for the MIS diode consist of a 5000-Å-thick n^+ GaAs contact layer doped with Si to 2×10^{18} cm^{-3} on a semi-insulating GaAs substrate, a 5000-Å-thick n-type GaAs active layer doped to 5×10^{16} cm^{-3}, a 100-Å-thick undoped AlAs barrier layer, an LTG insulating layer with various thickness and material composition, another 100-Å-thick undoped AlAs barrier layer, and finally, a 50-Å-thick undoped GaAs cap layer. All the layers except the LTG insulator were grown at 600 °C. The growth temperature for the LTG insulator, ranging from 200 to 350 °C, is specified in the next section for each particular diode. The n-type GaAs layer corresponds to the conducting channel in a MISFET and all the layers above it are treated as the gate insulator. As for the MISFET structure used in the TEM study, the GaAs caps and all the AlAs barriers are 200 Å thick and the n-type active layer is 1000 Å thick and doped to 2×10^{17} cm^{-3}. The thicknesses for the LTG-GaAs gate insulator and the LTG-GaAs buffer, all were grown at 200 °C, are 800 Å and 5000 Å, respectively.

After growing the LTG insulator and prior to the growth of the top AlAs barrier, the wafer was annealed at 600 °C for 10 min in the growth chamber. Fabrication of the diode starts by forming 150-μm-diameter Ti/Au dots using photoresist lift-off. Diode isolation was accomplished by wet etching to the n^+ GaAs contact layer using the Ti/Au metallization

as the self-aligned etch mask. Then a Ni/Ge/Au metallization was deposited on the contact layer and alloyed to form the cathode of the diode. MISFETs were fabricated on the wafer used for the TEM study and the fabrication process was described in Ref. 4.

IV. Experimental Results and Discussion

A. TEM study of an LTG-GaAs MISFET Structure

The photographs in Fig. 2 are the cross-sectional TEM images of an as-grown sample and the same sample after rapid thermal anneal (RTA). The RTA was done at 800 °C for 10 s using a GaAs substrate as the proximity cap. Throughout this paper the term "annealing" is referred to this RTA process which is suitable for implant activation. All the LTG samples have been annealed at 600 °C for 10 min in-situ before being taken out of the MBE growth chamber for process.

The As precipitates are uniformly distributed in the LTG GaAs layers in both the as-grown and the annealed samples, and they are not found in the normal GaAs layers below or above the LTG GaAs insulator. The average diameters of the As precipitates are 35 Å in the as-grown sample and 115 Å in the annealed sample which are consistent with previously reported results [12]. Because there are no As precipitates in the top GaAs cap layer and no sign of precipitate diffusion in the LTG GaAs layer, it is believed that the properties of the LTG GaAs are the same throughout the layer and the loss of As precipitates upon RTA is negligible. Although thinner, 100-Å-thick AlAs barriers were used in our MIS diode structure, they should still be effect barriers based on the current TEM results and previously published data [11].

B. Diodes with an 800-Å-thick insulator

Diodes were fabricated with an 800-Å-thick LTG GaAs insulator grown at either 200 °C or 350 °C. Because an Al_3Ga_7As insulator grown at 300 °C has a resistivity much higher than any LTG GaAs [7], a third diode with an 800-Å-thick LTG $Al_{31}Ga_{69}As$ insulator was also fabricated. As shown in Fig. 3(a), before annealing the diode with LTG $Al_{31}Ga_{69}As$ insulator has the lowest gate current and the diode with the LTG GaAs grown at 350 °C has the highest. The current difference between each sample is approximately two orders of magnitude up to 2 V of forward bias. Because the resistivity is the highest for the LTG $Al_{31}Ga_{69}As$ grown at 300 °C [7] and the lowest for the LTG GaAs grown at 350 °C, the measured results suggest that the resistivity of the insulator

determines the forward-bias current. Another evidence that the LTG GaAs grown at lower temperature is more resistive is that the gate current of our diode with an 800-Å-thick LTG GaAs grown at 200 °C is comparable to that of a previously reported diode with an 2000-Å-thick LTG GaAs grown at 250 °C [6].

After the RTA the diode current increases for all samples. The current increases by a factor of five to six between 0 and 2 V of forward bias for diodes with an LTG GaAs insulator and the current for the diode with the LTG GaAs grown at 200 °C is still lower than that with LTG GaAs grown at 300 °C. As for the LTG $Al_{.31}Ga_{.69}As$ diode, after the RTA the current increases by two to three orders in the same voltage range and the current becomes comparable to that for the LTG GaAs diodes after the same RTA. It is known that the high bonding energy of Al to As makes it more difficult for the excess As to form precipitates in the LTG AlGaAs than in the LTG GaAs, and the size of the As precipitates is also less likely to grow quickly upon high-temperature treatment [12]. Therefore, a possible explanation for the more severe degradation of the LTG $Al_{.31}Ga_{.69}As$ is that the RTA effectively reduced the density of the deep traps while the formation and the growth of the As precipitates lagged, resulting in a fast reduction in resistivity. The experimental results are consistent with the theory that both defect-related deep traps and As precipitates contribute to the high resistivity of the LTG materials.

As shown in Fig. 4 the reverse-biased diode current is less sensitive to the type of LTG material than the forward-bias current and does not increase significantly after annealing. The main reason is that under the reverse-bias condition, a depletion region is formed in the n-type normal GaAs layer underneath the gate insulator and a significant portion of the applied negative voltage drops across this region. Because the breakdown strength of the LTG material is usually larger than that of the normal GaAs, reverse breakdown is most likely to take place in the doped GaAs layer. Consequently, the reverse-biased current or the breakdown voltage is less sensitive to the change of properties of the LTG insulator after annealing. The result also suggests that in an actual MISFET, the doping concentration of the channel and other physical parameters, such as the channel thickness and gate-drain spacing, would play a more important role in determining the reverse breakdown voltage.

In a digital circuit the forward-bias gate voltage of a MISFET, at which the acceptable maximum gate current is reached, determines the allowable voltage swing and the stand-by power consumption and is one of the most important parameters to optimize. In order to evaluate the quality of various LTG insulators for low gate-current MISFET

applications, the turn-on voltage, defined here as the forward-bias voltage at which the diode current reaches 1 nA per μm^2 diode area, was measured and listed in Table I. The temperature in the parenthesis following a material specifies its growth temperature and the item "ΔV" is the amount of the voltage decrease after the annealing. Referring to Table I the 3.71-V of the turn-on voltage before the RTA is the highest and was measured on the diode with the LTG $Al_{.31}Ga_{.69}As$ insulator. However, after the annealing the highest turn-on voltage among all the diodes decreased to 1.81 V and was obtained on the diode with the LTG GaAs grown at 200 °C. The turn-on voltage for the diode having the LTG $Al_{.31}Ga_{.69}As$ insulator, which was the highest before the RTA, was reduced by more than 60% to 1.31 V after the annealing. The breakdown voltages, defined at 1 mA of the reverse-biased current for the 150-μm-diameter diode, are also included in Table I and they did not change much with the annealing.

Next, the importance of the AlAs barrier layer above the LTG GaAs during the annealing was studied. Two samples from each of the two wafers having the LTG GaAs insulator were first etched to selectively remove the top GaAs cap and the AlAs barrier. After annealing one of the two samples from each wafer, diodes were made on all four samples in the same way described in the previous section. Table I shows that for the diode having the LTG GaAs grown at 200 °C before the RTA, the turn-on voltage was 2.41 V for unetched and 2.33 V for the sample (marked by 'No AlAs' in Table I) with the GaAs cap and the top AlAs barrier removed. This small voltage decrease indicates that the low diode-current in this type of MIS structure can be attributed mostly to the LTG insulator and that the wide-bandgap AlAs barrier layer may play only a minor role.

After the RTA the current of the diodes having the LTG GaAs insulator and the top AlAs barrier is approximately ten times lower than that of the diode with the top AlAs barrier removed. As shown in Table I, the decrease of the turn-on voltage as the result of the RTA is always larger for the diode with the top AlAs barrier etched. This comparison suggests that without the AlAs layer on top of the LTG GaAs insulator, a fair amount of the excess As may have been lost during the annealing, resulting in a large increase of the diode current. Again, the change of the diode current under reversed bias is smaller.

C. Diodes with a 300-Å-thick insulator

In this part of the work the thickness of the LTG AlGaAs insulator was reduced to 300 Å while the thicknesses of the other epitaxial layers were kept the same. For a semiconductor the resistivity generally increases with the bandgap. Therefore, the LTG

AlGaAs with an Al mole fraction of 43% (which gives rise to the highest direct-bandgap energy) was used as the insulator in addition to the LTG AlGaAs with 31% Al discussed earlier. Since the LTG AlGaAs grown at lower temperatures has a higher resistivity [7], MIS diodes with LTG $Al_{.43}Ga_{.57}As$ insulator grown at both 250 °C and 300 °C were compared. For 31% of Al mole fraction, only the LTG $Al_{.31}Ga_{.69}As$ layer grown at 300 °C was studied. Another $Al_{.31}Ga_{.69}As$ layer was grown at the normal 600 °C which is used as the control sample to evaluate the improvement the LTG AlGaAs layers provide.

Measured forward-biased currents for diodes with various AlGaAs layer are shown in Fig. 5. Comparing to Fig. 3(a), one can see that by reducing the thickness of the LTG $Al_{.31}Ga_{.69}As$ grown at 300 °C from 800 to 300 Å, the current increases by approximately three orders of magnitude up to 2 V of forward bias. As shown in Fig. 5(a), an increase of the Al mole fraction from 31% to 43% at the same growth temperature of 300 °C lowers the gate current of the diode only slightly without the RTA. However, decreasing the growth temperature of the $Al_{.31}Ga_{.69}As$ from the normal 600 °C to the 300 °C in the low-temperature-growth regime reduced the current significantly. In the low-temperature-growth regime additional current reduction can be achieved by lowering the growth temperature further from 300 to 250 °C, as depicted by the curves for the diodes with the $Al_{.43}Ga_{.57}As$ insulator shown in Fig. 5(a).

The currents for the same group of diodes after the RTA are plotted in Fig. 5(b). First, the effect of the growth temperature of the AlGaAs layer is examined. In the low-growth-temperature regime with 43% Al mole fraction, the current for the diode with $Al_{.43}Ga_{.57}As$ grown at 250 °C increased dramatically while the current increased more modestly for the diode with the $Al_{.43}Ga_{.57}As$ grown at 300 °C. Actually, the current for the diode with $Al_{.43}Ga_{.57}As$ grown at 250 °C becomes higher than that with $Al_{.43}Ga_{.57}As$ grown at 300 °C, a reversal of the results before the RTA. For 31% Al mole fraction, the current increase for diodes with LTG $Al_{.31}Ga_{.69}As$ grown at 300°C insulator is also significant while the current changes very little for diodes with the normal $Al_{.31}Ga_{.69}As$ grown at 600 °C. Although the Al mole fractions are not the same for all the AlGaAs insulators studied, the result reveals the trend that the degree of the property change after the RTA increases with decreasing growth temperature.

For the same 300 °C growth temperature the current of the diode having the $Al_{.31}Ga_{.69}As$ with 31% Al increased significantly after RTA while the current of the diode having the $Al_{.43}Ga_{.57}As$ with 43% Al hardly changed. By comparison, the current of the diode with the $Al_{.43}Ga_{.57}As$ insulator grown at 300 °C measured in this work is

approximately four orders of magnitude lower than the gate current of a MISFET with an Al_5Ga_5As insulator grown at the normal temperature reported previously [15]. Both of these samples have gone through a similar RTA process and the thicknesses for the Al_5Ga_5As in Ref. 15 and the $Al_{43}Ga_{57}As$ in our diode are 600 Å and 300 Å, respectively. The advantage of growing the AlGaAs with a high Al content at low temperatures becomes obvious.

All the measured data for diodes with a 300-Å AlGaAs insulator are listed in Table II with the same parameters used in Table I. Results shown in Table II indicate that the AlGaAs layer becomes less sensitive to the RTA with a higher growth temperature. A turn-on voltage of 2.57 V was measured for the diode with the $Al_{43}Ga_{57}As$ grown at 250 °C and is the highest among all diodes. However, this turn-on voltage drops more than 50% to 1.12 V after the RTA and is lower than the 1.42 V for the diode with the $Al_{43}Ga_{57}As$ grown at 300 °C. The turn-on voltage for the diode with the $Al_{31}Ga_{69}As$ grown at the normal 600 °C did not decrease much after the RTA but it was always higher than those for the diodes with the LTG $Al_{31}Ga_{69}As$. Although the LTG AlGaAs and GaAs layers grown at a very low temperature may appear to be ideal if no annealing is required in the process, the long-term reliability issue should be addressed due to their poor thermal stability.

On two samples having an $Al_{43}Ga_{57}As$ insulator grown at 300°C, the top GaAs cap and the AlAs barrier were etched. The current increase after the RTA is approximately two orders of magnitude higher than that with the top AlAs barrier. It appears that the presence of the AlAs barrier during the high-temperature annealing is equally important to the LTG AlGaAs as to the LTG GaAs. The difference of the reverse-biased current before and after the RTA for all the diodes with AlGaAs insulators is small.

IV. Conclusion

The dependence of the current on the LTG GaAs and AlGaAs insulators in an MIS diode similar to the gate structure of a MISFET was studied. The amount of the forward-biased-current increase after the RTA varies widely with the type of the insulator. On the other hand, the reverse-bias current does not change much after annealing and is not sensitive to the type of the insulator. The added AlAs barrier on top of the LTG insulator appears to prevent the outdiffusion of the excess As in the LTG insulator and, thus, alleviate the degradation of the resistivity during the RTA.

In conclusion, when used as the insulator, the LTG GaAs and AlGaAs layers show significant improvement compared to the commonly used normal AlGaAs in reducing the forward-biased diode current and both the LTG GaAs and LTG AlGaAs could be used satisfactorily as the MIS gate insulator in a self-aligned MISFET. Because of the vast variation of their properties, the type of the LTG insulator and the growth temperature should be optimized for specific device and process requirements. For all the insulating layers we tested, the LTG GaAs grown at 200 °C and the LTG $Al_{.43}Ga_{.57}As$ grown at 300 °C yielded the lowest diode current after the RTA similar to that used for implant activation. On the other hand, if no high-temperature annealing is required for device fabrication, the $Al_{.43}Ga_{.57}As$ grown at even lower 250 °C is the insulator for the lowest diode current.

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Figure Captions

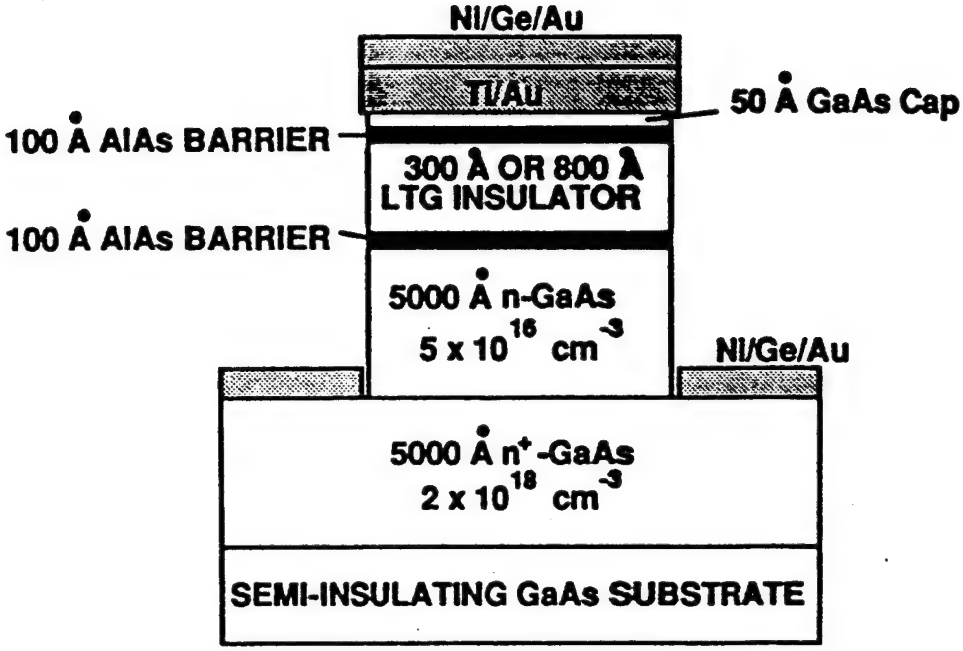
Fig. 1 Layer structure of the MIS diode.

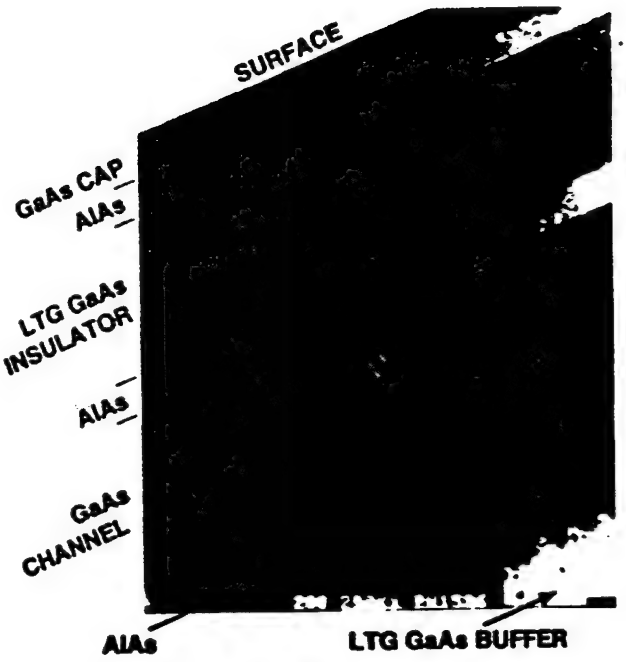
Fig. 2 Cross sectional TEM of an LTG GaAs gate layer sandwiched by AlAs barriers. All the layers were grown at 600 °C except for the LTG GaAs which was grown at 200 °C. The thickness for all the AlAs layers and the GaAs cap layers is 200 Å. The LTG GaAs insulator is 800 Å thick, the GaAs channel is 1000 Å thick, and the LTG GaAs buffer is 5000 Å thick. Notice that there is no As precipitates in the GaAs cap layer. (a) Before annealing. (b) After annealing.

Fig. 3 Measured forward-biased current of diodes with an 800-Å-thick insulator. (a) Before annealing. (b) After annealing.

Fig. 4 Measured reverse-biased current of diodes with an 800-Å-thick insulator. (a) Before annealing. (b) After annealing.

Fig. 5 Measured current of diodes with an 300-Å-thick LTG AlGaAs insulator. (a) Before annealing. (b) After annealing.

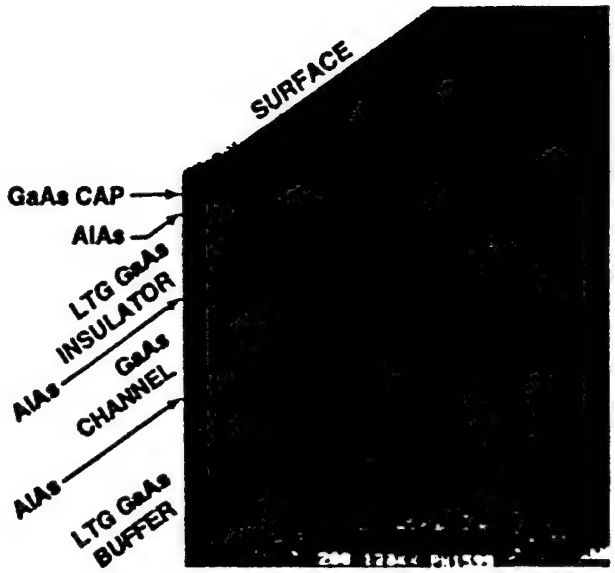

Ni/Ge/Au
Ti/Au
50 Å GaAs Cap
100 Å AlAs BARRIER
300 Å OR 800 Å
LTG INSULATOR
100 Å AlAs BARRIER
5000 Å n-GaAs
5 x 10^16 cm^-3
Ni/Ge/Au
5000 Å n+-GaAs
2 x 10^18 cm^-3
SEMI-INSULATING GaAs SUBSTRATE


SURFACE
GaAs CAP
AlAs
LTG GaAs
INSULATOR
AlAs
GaAs
CHANNEL
AlAs
LTG GaAs BUFFER

(a)

254058-7

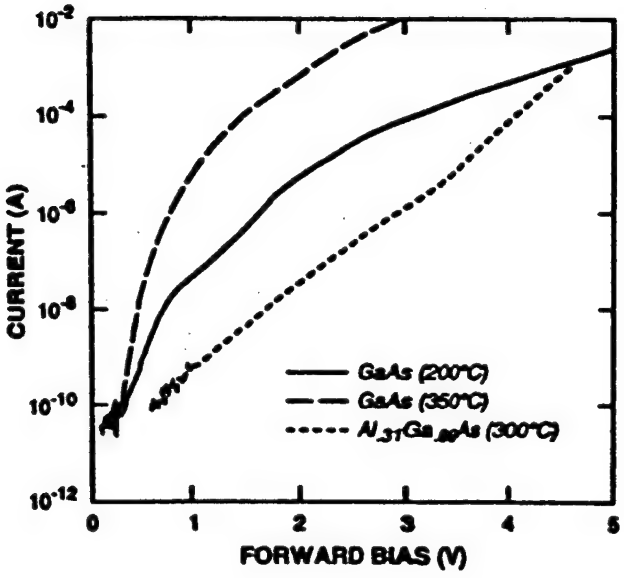
2(a)



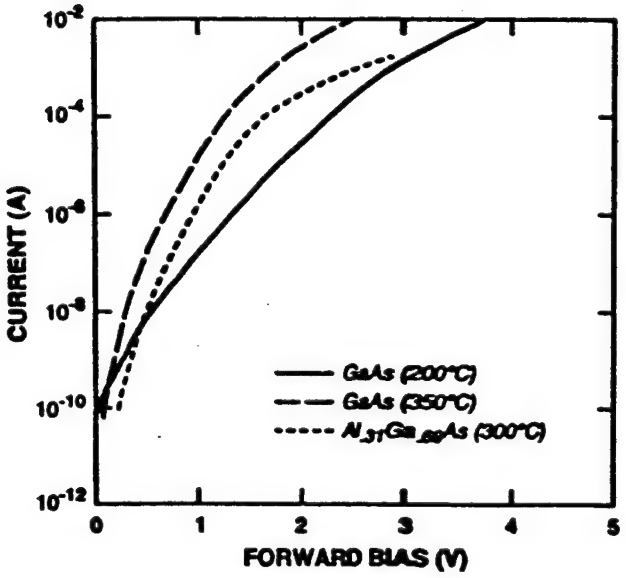
(b)

251811-14

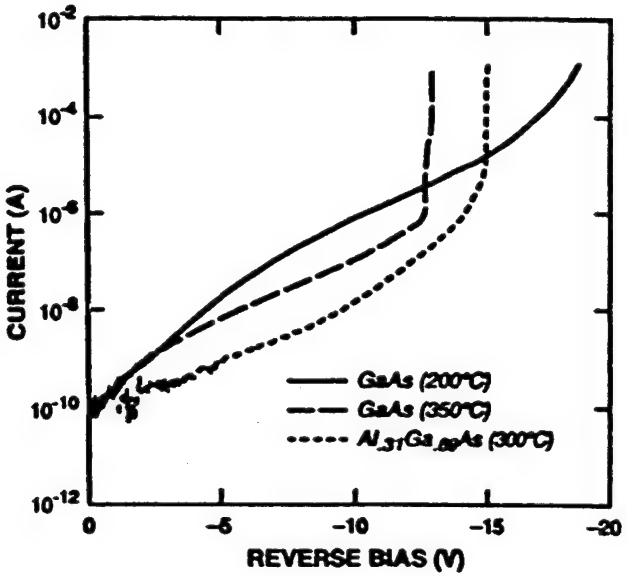
2(b)


CURRENT (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
0
1
2
3
4
5
FORWARD BIAS (V)
GaAs (200°C)
GaAs (350°C)
$Al_{.31}Ga_{.69}As$ (300°C)

254668-4


CURRENT (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
0
1
2
3
4
5
FORWARD BIAS (V)
GaAs (200°C)
GaAs (350°C)
$Al_{.31}Ga_{.69}As$ (300°C)

254859-2


10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
CURRENT (A)
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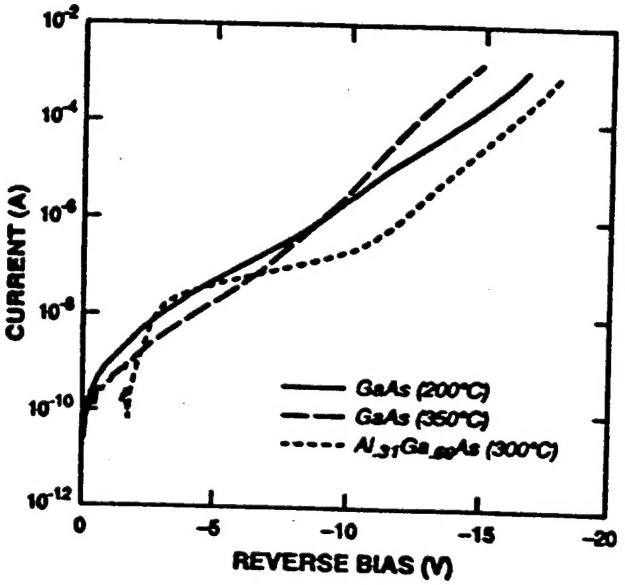
−5
−10
−15
−20
REVERSE BIAS (V)
GaAs (200°C)
GaAs (350°C)
$Al_{.31}Ga_{.69}As$ (300°C)

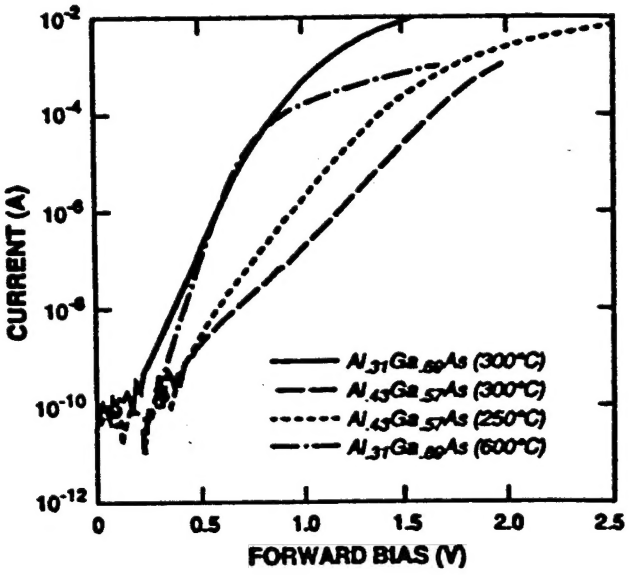
254058-3

4(a)


10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
CURRENT (A)
0
−5
−10
−15
−20
REVERSE BIAS (V)
GaAs (200°C)
GaAs (350°C)
$Al_{.31}Ga_{.69}As$ (300°C)

254058-1

4(b)


CURRENT (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
0
0.5
1.0
1.5
2.0
2.5
FORWARD BIAS (V)
$Al_{.31}Ga_{.69}As$ (300°C)
$Al_{.43}Ga_{.57}As$ (300°C)
$Al_{.43}Ga_{.57}As$ (250°C)
$Al_{.31}Ga_{.69}As$ (600°C)

254058-6

TABLE I Measured voltages for diodes with 800 Å LTG GaAs and AlGaAs

Devices	Forward Turn-on @1 nA/μm², V			Reverse Breakdown @1 mA, V	
	No Anneal	Annealed	ΔV	No Anneal	Annealed
LTG GaAs (200 °C)	2.41	1.81	.60	19.0	16.0
LTG GaAs (350 °C)	1.17	1.09	.08	14.0	13.0
LTG GaAs (200 °C) No AlAs	2.33	1.46	.87	18.0	16.5
LTG GaAs (350 °C) No AlAs	1.13	.89	.24	15.0	15.2
LTG $Al_{31}Ga_{69}As$ (300 °C)	3.71	1.31	2.46	15.5	17.5

TABLE II Measured voltages for diodes with 300 Å AlGaAs

Devices	Forward Turn-on @1 nA/μm², V			Reverse Breakdown @1 mA, V	
	No Anneal	Annealed	ΔV	No Anneal	Annealed
LTG $Al_{.31}Ga_{.69}As$ (300 °C)	1.45	0.75	0.70	14.3	16.5
LTG $Al_{.43}Ga_{.57}As$ (300 °C)	1.59	1.42	0.17	16.0	15.4
LTG $Al_{.43}Ga_{.57}As$ (250 °C)	2.57	1.12	1.45	17.7	18.8
$Al_{.31}Ga_{.69}As$ (600 °C)	0.62	0.59	0.03	18.6	18.7